

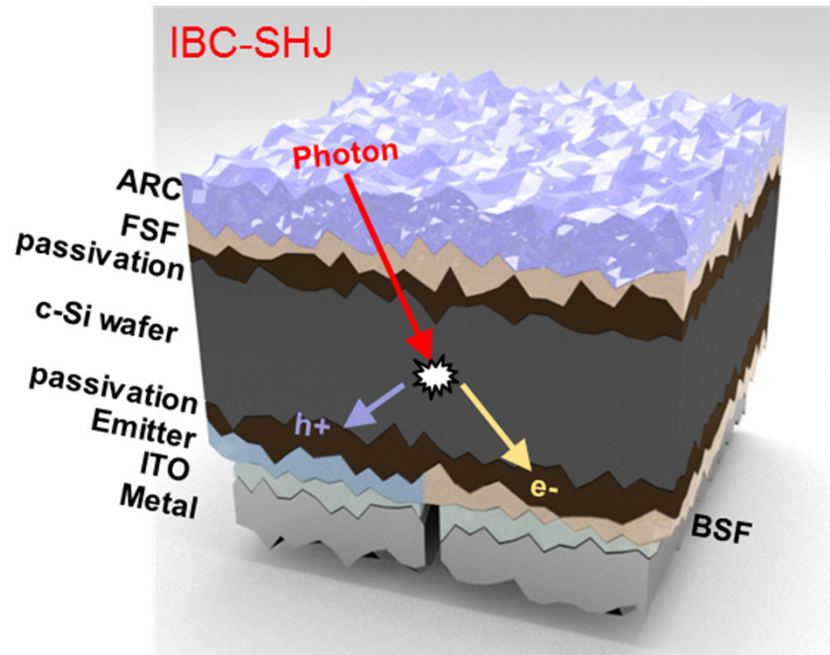
NextBase project (Next-generation interdigitated back-contacted silicon heterojunction solar cells and modules by design and process innovations)

European workshop on nanotechnologies & advanced materials for PV & CSP,
24-25 October 2017, Brussels

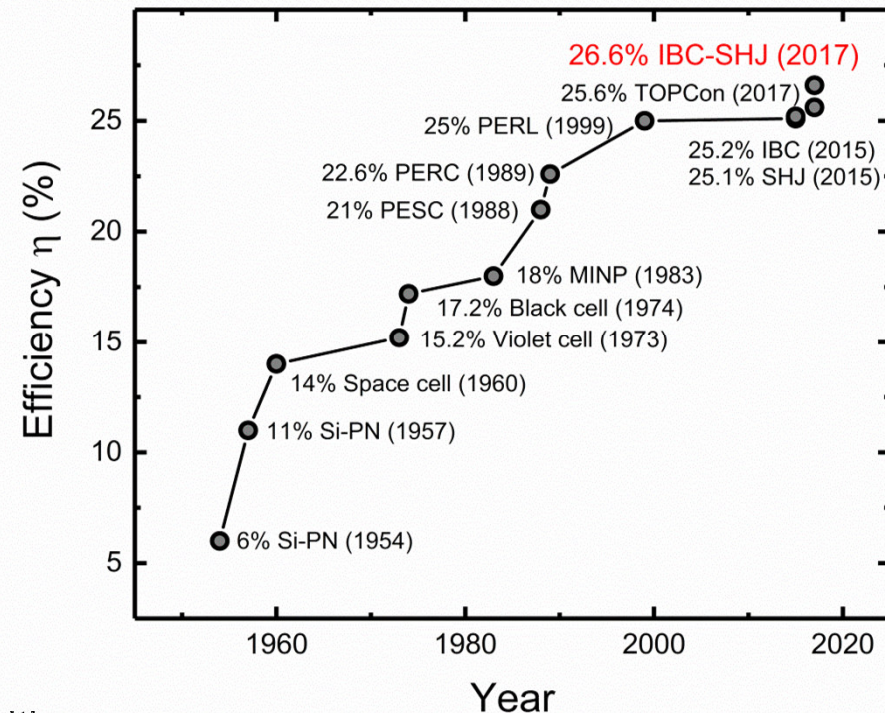
Dr. Kaining Ding, Forschungszentrum Jülich GmbH, Institut für Energie- und
Klimaforschung 5 - Photovoltaik



IBC-SHJ solar cell

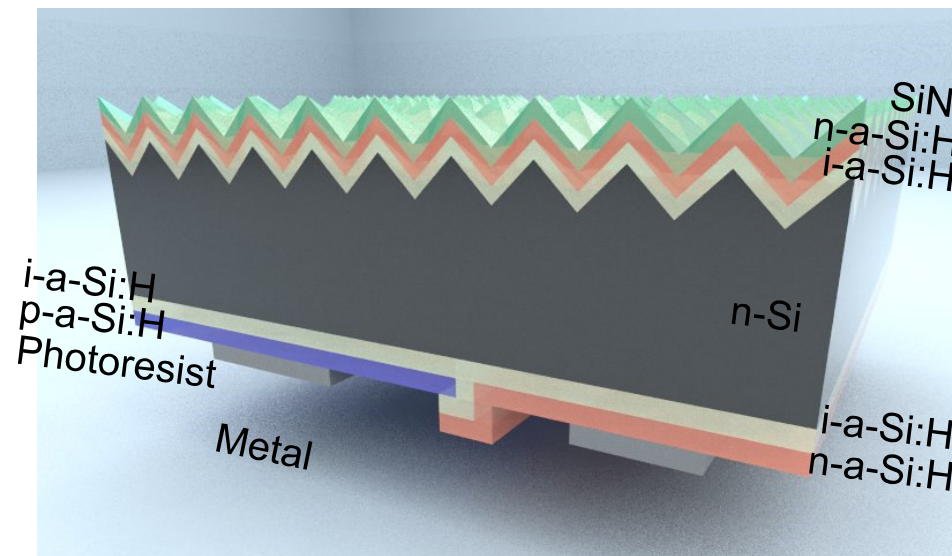


- Key advantage of IBC-SHJ solar cell
 1. SHJ: excellent surface passivation with intrinsic a-Si:H → high V_{oc}
 2. IBC: No metallization shading loss and no front TCO → high J_{sc}
 3. IBC + SHJ: combination of both advantages → high efficiency!



Fabrication of IBC-SHJ solar cell

- Patterning of rear side is complex and expensive
- Details of 26.6% record IBC-SHJ solar cell undisclosed



European effort to disclose the secrets of IBC-SHJ and to develop cost competitive and high efficiency IBC-SHJ technologies for European market

General Information



Project acronym: NextBase

Grant agreement number: 727523

Work programme: LCE-07-2016-2017

Starting date: 01.10.2016

End date: 30.09.2019

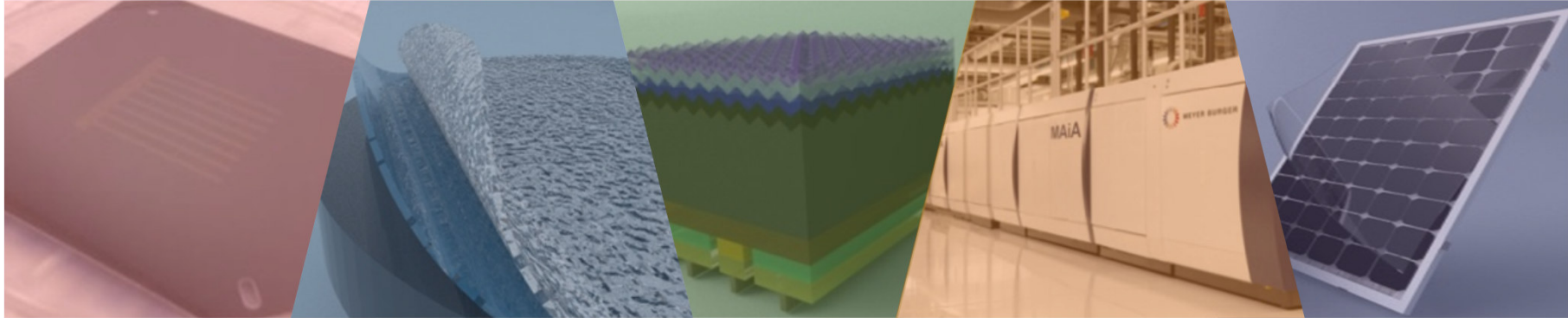
Budget: 5,7M€

Grant: 3,8M€

Coordinator: Dr. Kaining Ding (JÜLICH), k.ding@fz-juelich.de

Website: <http://nextbase-project.eu/>

Objectives



- Demonstrate IBC-SHJ solar cells with efficiency $> 26.0\%$.
 - Production of highest quality wafers with lifetime over resistivity ratio $> 2 \text{ ms/Ohmcm}$.
 - Introduction of transparent front stack and advanced light management for $J_{sc} > 42 \text{ mA/cm}^2$
 - Development of novel contact materials and contact designs for fill factor (FF) $> 82\%$ and $V_{oc} > 740 \text{ mV}$.
- Demonstrate IBC-SHJ solar modules with efficiency $> 22.0\%$.
 - Development of 60-cell interconnection and anti-reflection coating (ARC) for cell-to-module (CTM) ratio $> 95\%$.
 - Implementation of encapsulation with relative power decrease $< 5\%$ after degradation.
- Develop an industrial prototype PECVD reactor for IBC-SHJ solar cells.
 - Production of 6-in wafer with lifetime $> 2\text{ms}$ with patterned doped layer.
 - Demonstration of minimum throughput of 10 wafers per hour.
- Develop processes that allow IBC-SHJ solar module cost of $< 0.35 \text{ €/W}_p$.
 - Development of high quality n-type wafers by low-cost multi-pulling process.
 - Development of various cost competitive patterning and interconnection techniques.

Work package structure

WAFER

- Wafer specification
- Thermal process
- Single-side texturing
- Advanced texture

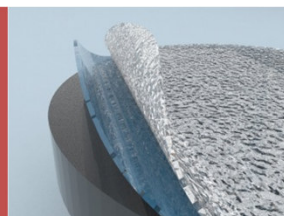


Cost & Life-cycle Analysis

- Cost assessment
- Scale-up analysis
- Environmental
- System impact

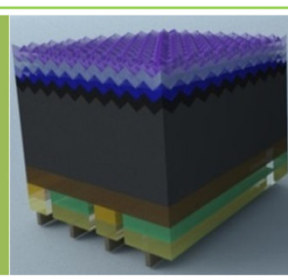
LAYER

- Rear contact material
- Transition metal oxide
- Front layer stack
- Electro-plated metal



CELL

- Patterning techniques
- Light management
- 26% cell processing



TOOL

- Tool specification
- System validation
- Pilot cell fabrication



Characterization & Modeling

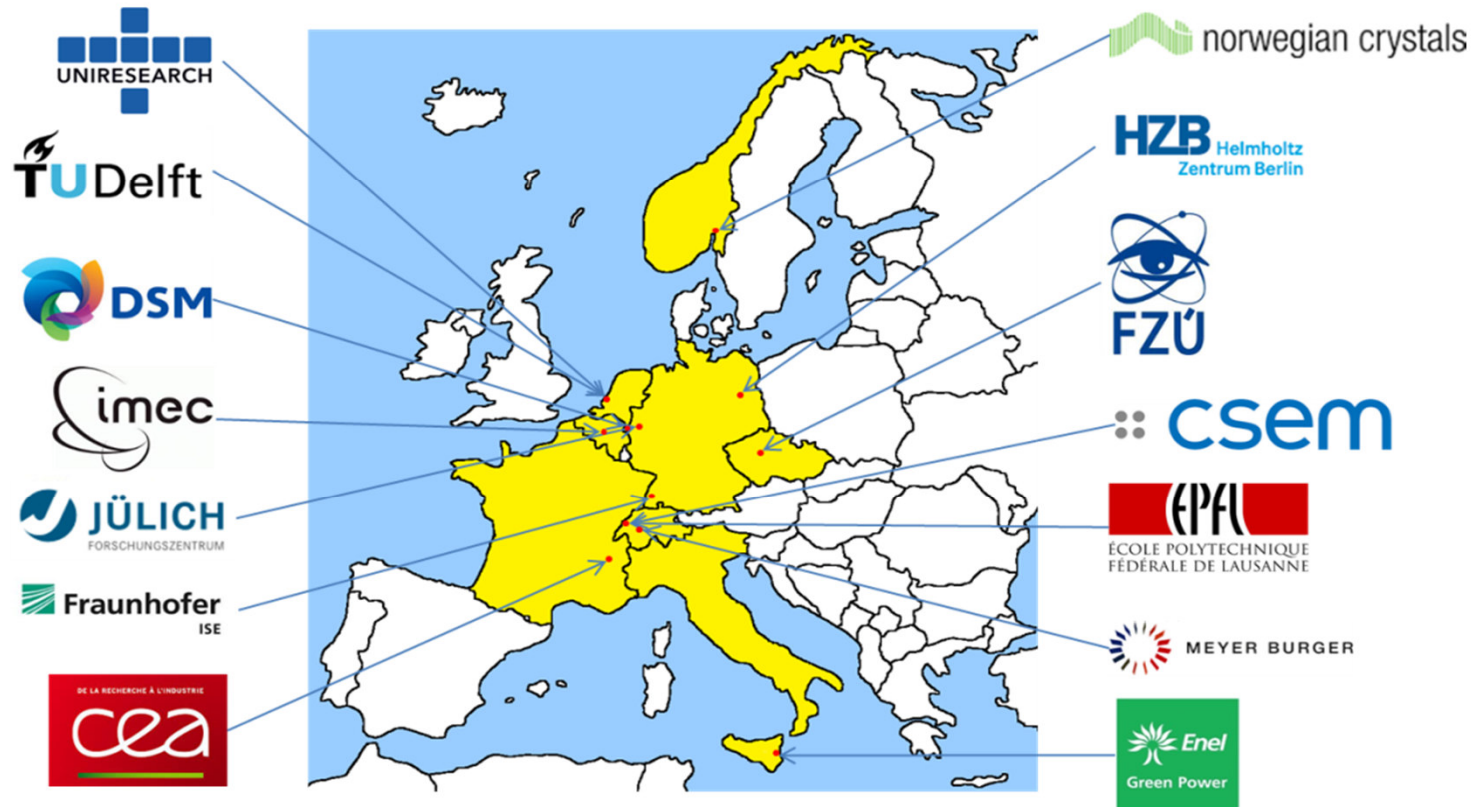
- Loss analysis
- Device simulation
- Measurement setup
- Module testing

MODULE

- Interconnection
- Encapsulation
- Anti-reflection coatings
- 22% module processing



Partners

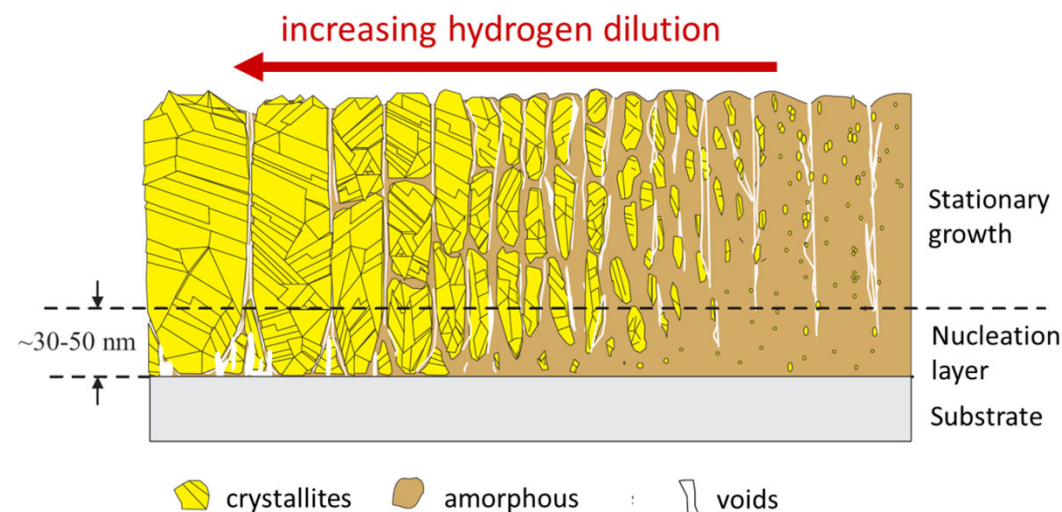
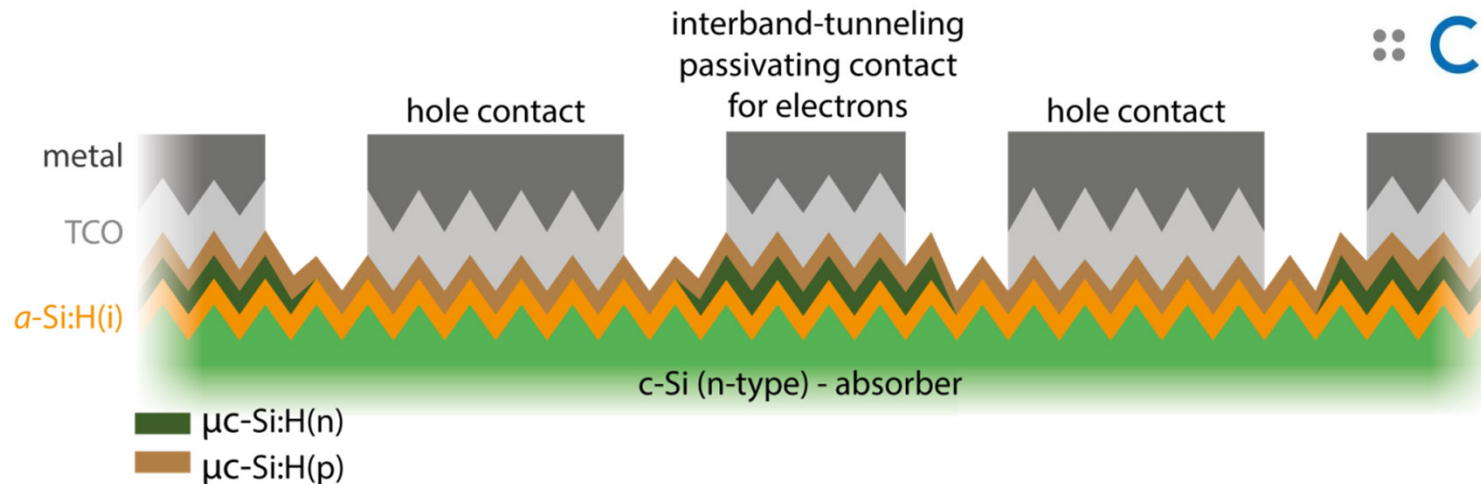


Brother/sister projects:

- DISC: passivated contact, <http://www.disc-project-h2020.eu/>
- AMPERE: SHJ production, <http://www.ampere-h2020.eu/>

Tunnel IBC with $\mu\text{c-Si}$

Shadow mask patterning with less alignment requirement



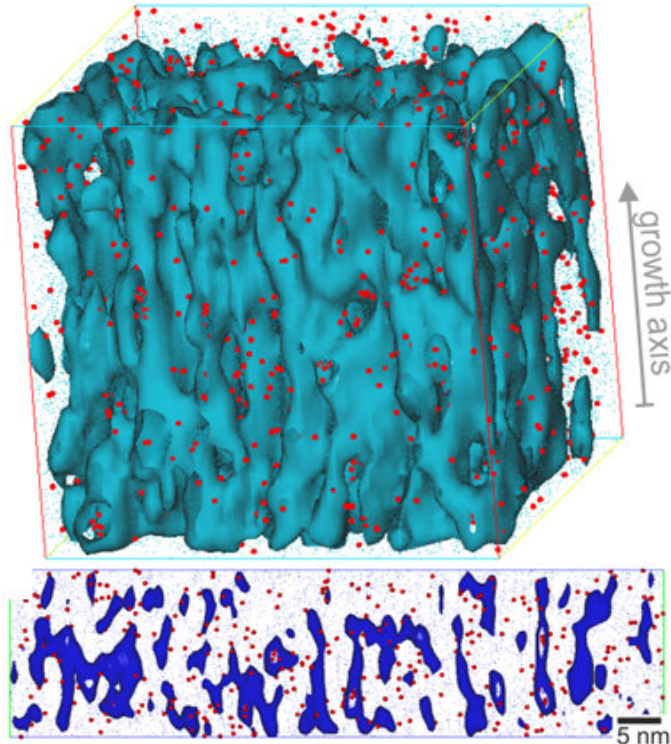
$\langle n \rangle \mu\text{c-Si:H}$ is highly conductive

23.9% efficient IBC-SHJ with tunnel IBC concept achieved!

Tomasi, A., et al. (2017) Nat. Energy, 2 (5), 17062.

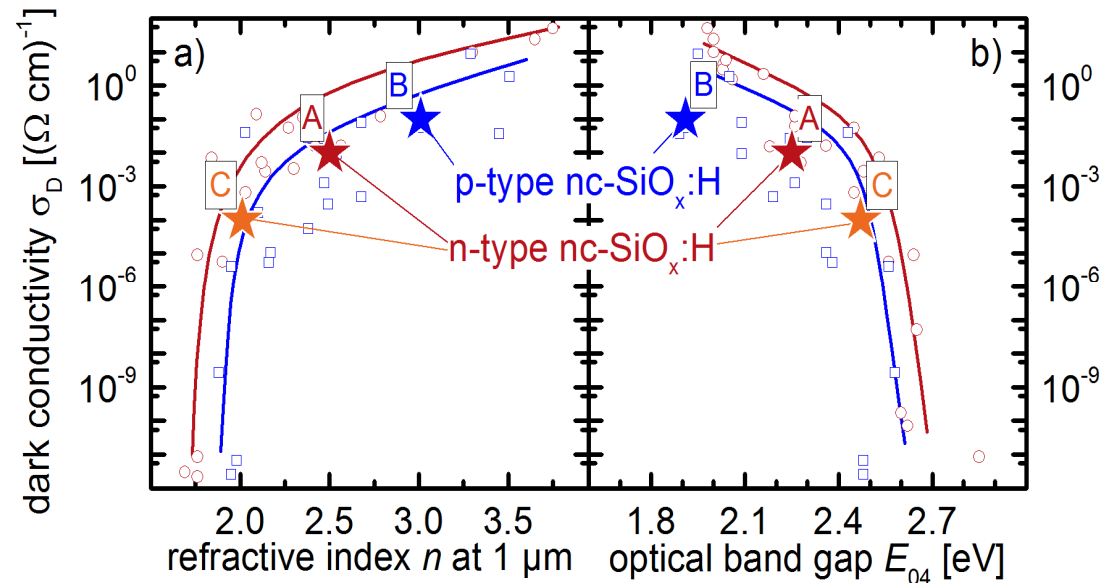
Nano-crystalline silicon oxide

Transparent and low refractive index contact layer



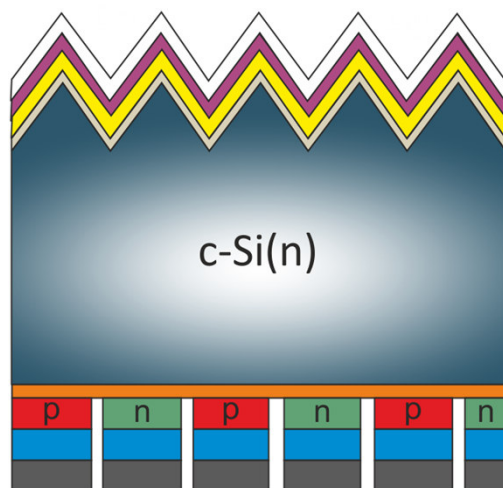
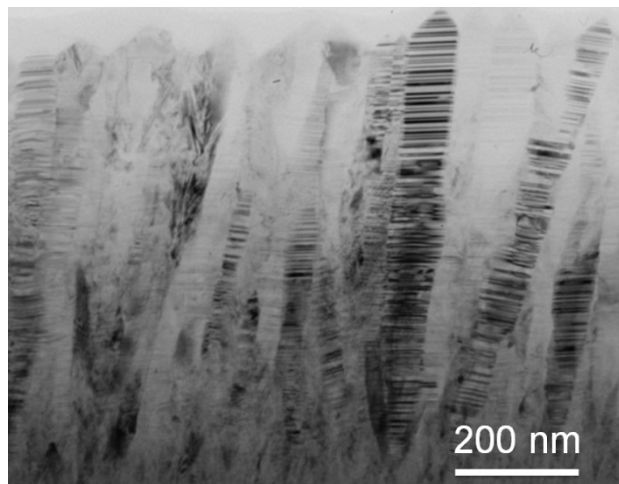
Advantages:

- Less parasitic absorption
- Better back reflection
- Less amorphous incubation
- More tuning options



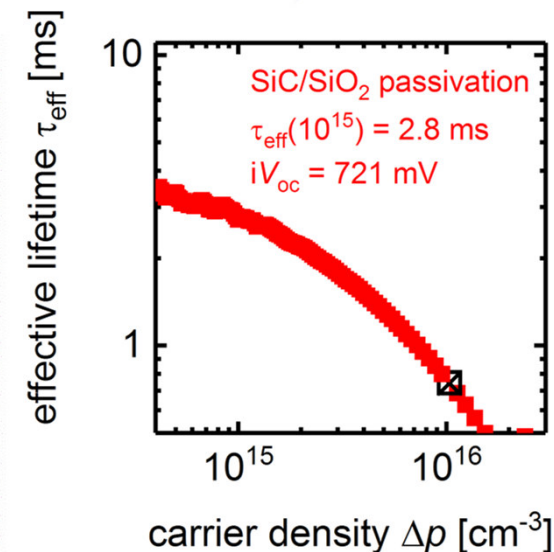
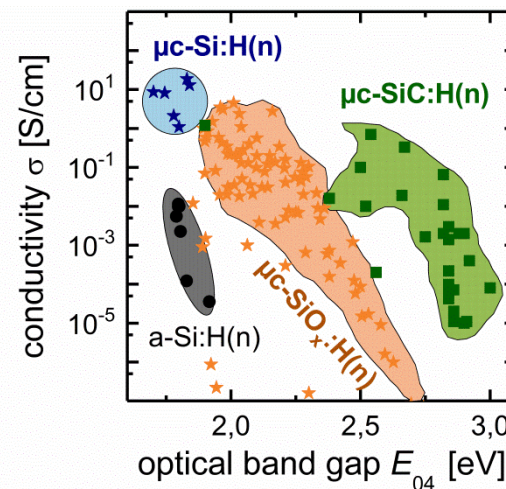
Nano-crystalline silicon carbide

Transparent front surface field



MgF₂
SiN_x
μc-SiC:H(n)
SiO₂

a-Si:H(i)
a-Si:H(n/p)
ITO
Ag



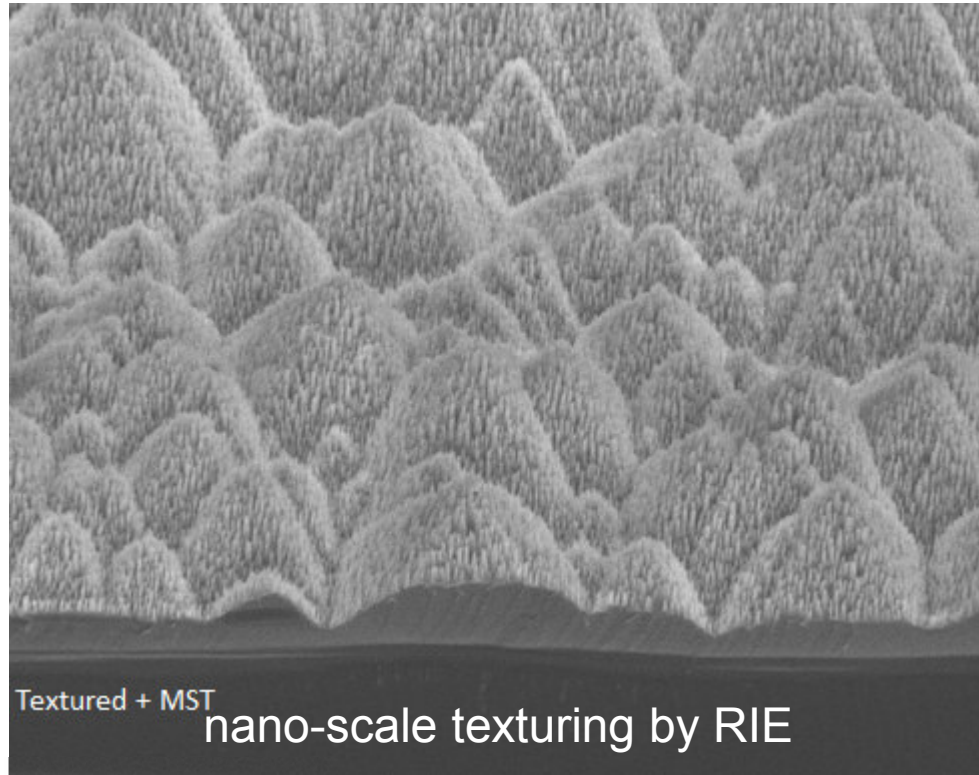
Advantages:

- Highly transparent SiO₂/SiC stack
- Refractive index matching
- High passivation quality
- Low-T process compatible with SHJ

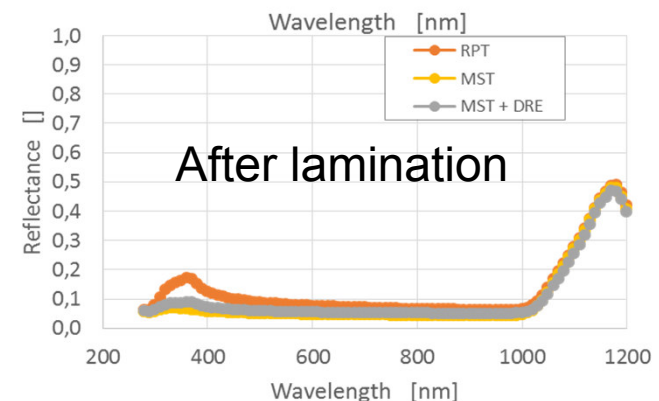
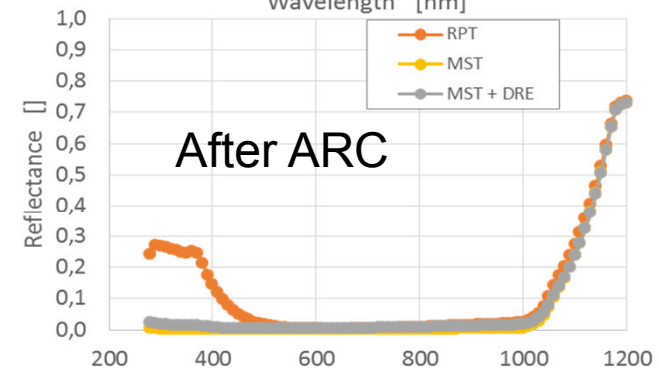
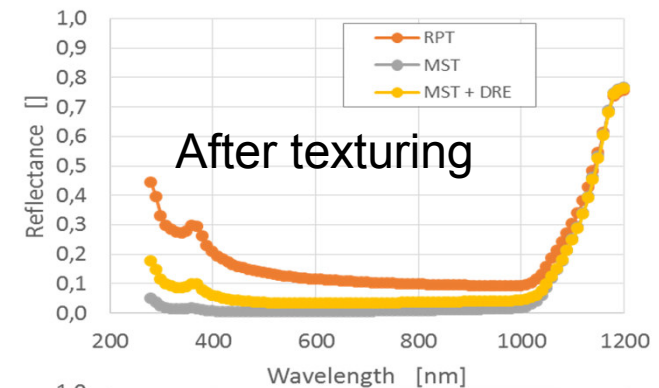
Ag M. Pomaska, et.al..(2015) Thin Solid Films, 595, 217–220.

Nano-size modulated surface texture

Broad-band light in-coupling and light scattering on front

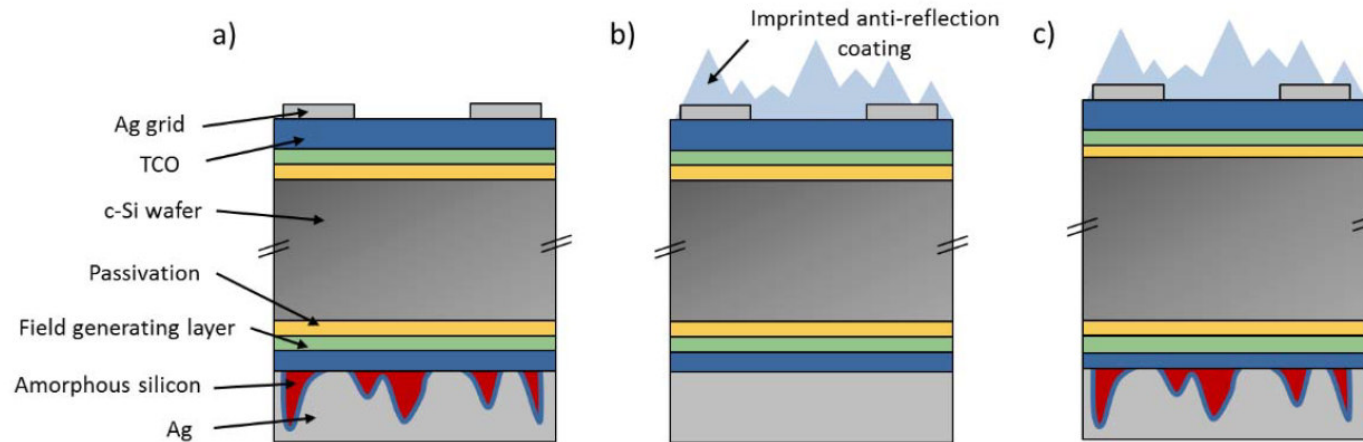


Lifetime above 1ms achieved after
damage remove etch (DER)!

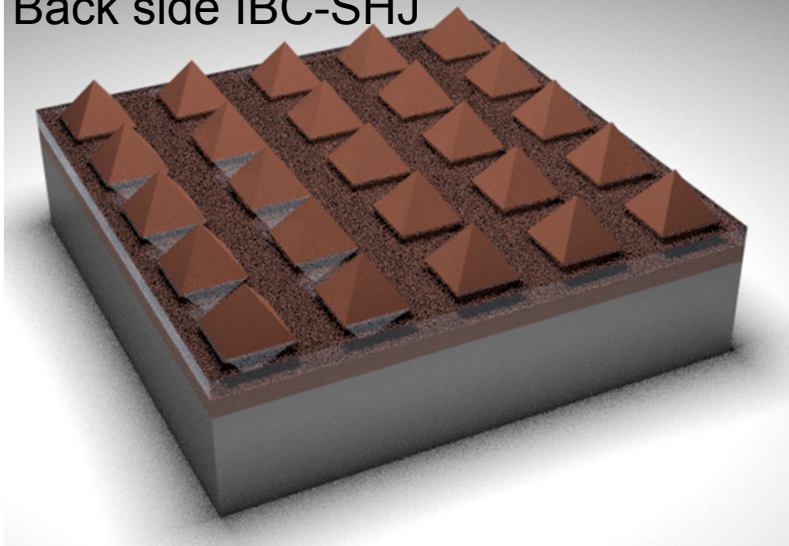


Nano-imprint structures

Post passivation light-management concepts



Back side IBC-SHJ



Advantages:

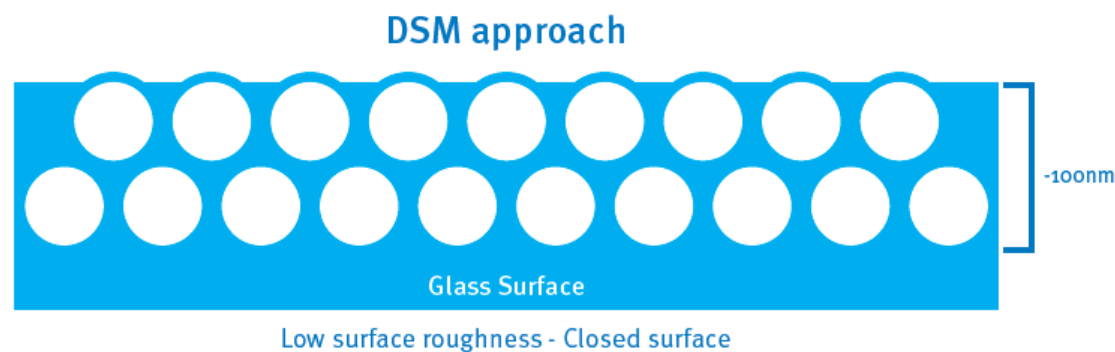
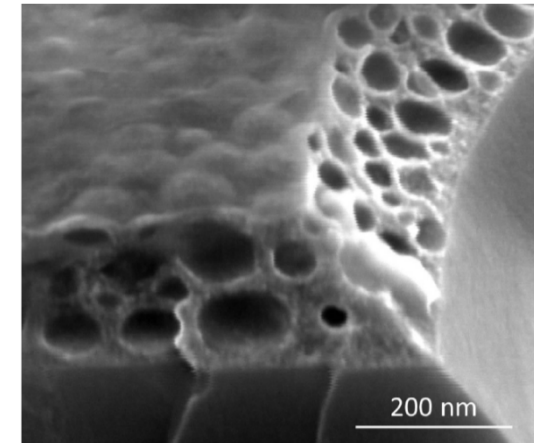
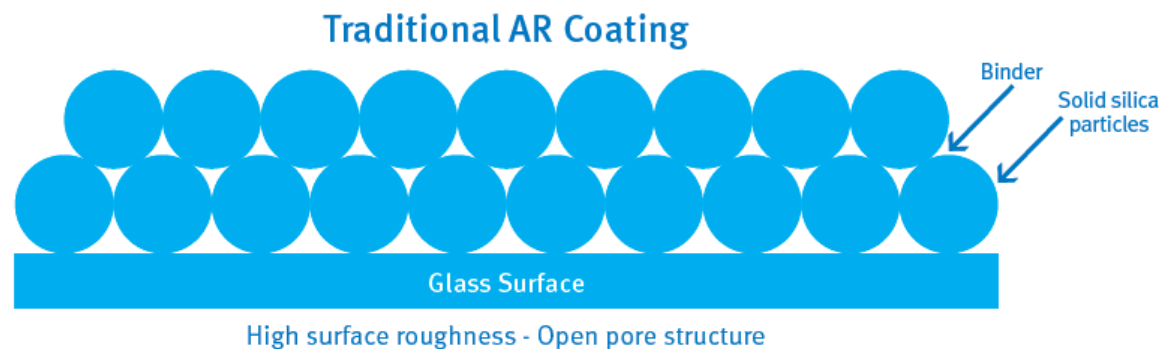
- Low cost process
- No harm to the passivation
- Flexible design of texture
- Ideal for thin wafers

Nano-porous AR coating

Refractive index matching for light incoupling



Single layer AR Coatings: Traditional versus Core-shell AR Coatings



Up to 4% less reflectance on module level at comparable fabrication cost at traditional AR coating

Acknowledgements



Thank you for your attention!



This project has received funding from the European Union's Horizon 2020 research and innovation programme under grant agreement No 727523

KPIs

Project KPI 3.1	Ingots of n-type Cz silicon with radial resistivity distribution in the range of +/-20% from target and oxygen content below 15 ppma.]
Project KPI 3.2	Implied photo-generated current density in targeted double- or single-side textured > 41.0 mA/cm ² .
Project KPI 4.1	Hole and electron contacts based on a-Si:H/nc-Si:H layers and TMOs with optimal specific contacting resistivity ($p_{\text{contact}} < 50 \text{ m}\Omega \cdot \text{cm}^2$) and contact passivation quality ($J_0 < 10 \text{ fA/cm}^2$).
Project KPI 4.2	IBC-SHJ front-side stack with optimal surface recombination velocity ($S_{\text{eff}} < 5 \text{ cm/s}$ under maximum power point conditions) and low absorption loss ($J_{\text{abs}} < 0.5 \text{ mA/cm}^2$).
Project KPI 5.1	IBC-SHJ devices processed with $V_{\text{oc}} > 740 \text{ mV}$, $\text{FF} > 82 \%$ and $J_{\text{sc}} > 42 \text{ mA/cm}^2$. IBC-SHJ device with efficiency $\geq 26.0\%$ on 6-in wafer.
Project KPI 6.1	Silicon doped layer thickness between 5 to 20 nm. Activation energy (E_a) < 0.4 eV for n and p doped layers.
Project KPI 6.2	6-in passivated wafer with patterned doped layer with lifetime level above 2 ms. Minimum throughput of 10 wa-fers per hour.
Project KPI 7.1	Module performance of higher than 22% and CTM power ratio of higher than 95%
Project KPI 7.2	Relative power decrease of less than 5% after 400 cycles of thermal cycle test (TCT) and 2000 h of damp heat