Crystalline Silicon Photovoltaics: Current Status and Future Challenges

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PUBLIC

Acknowledgements

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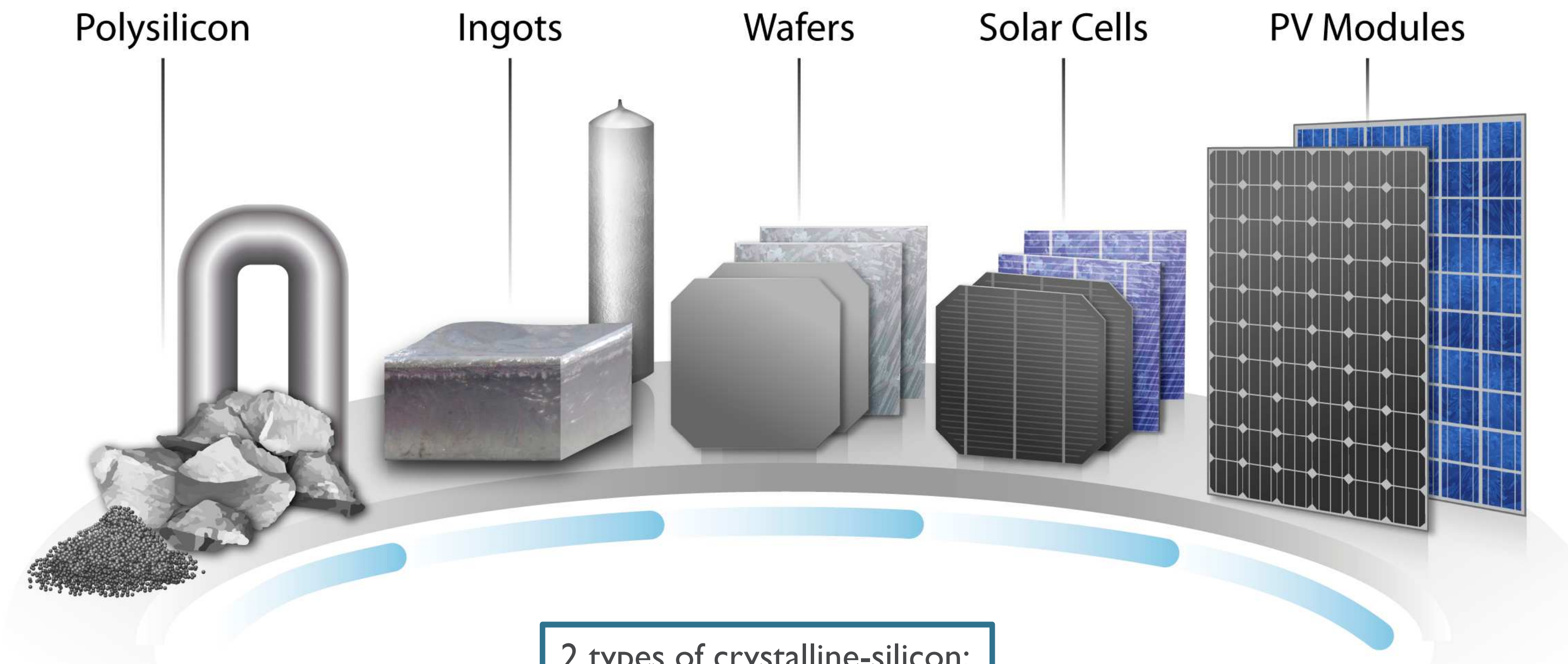
Outline

- Current production of silicon solar cells
- Novel cell structures for higher efficiencies
- Reducing material costs
- Tandem devices with silicon bottom cells

Current production of silicon solar cells

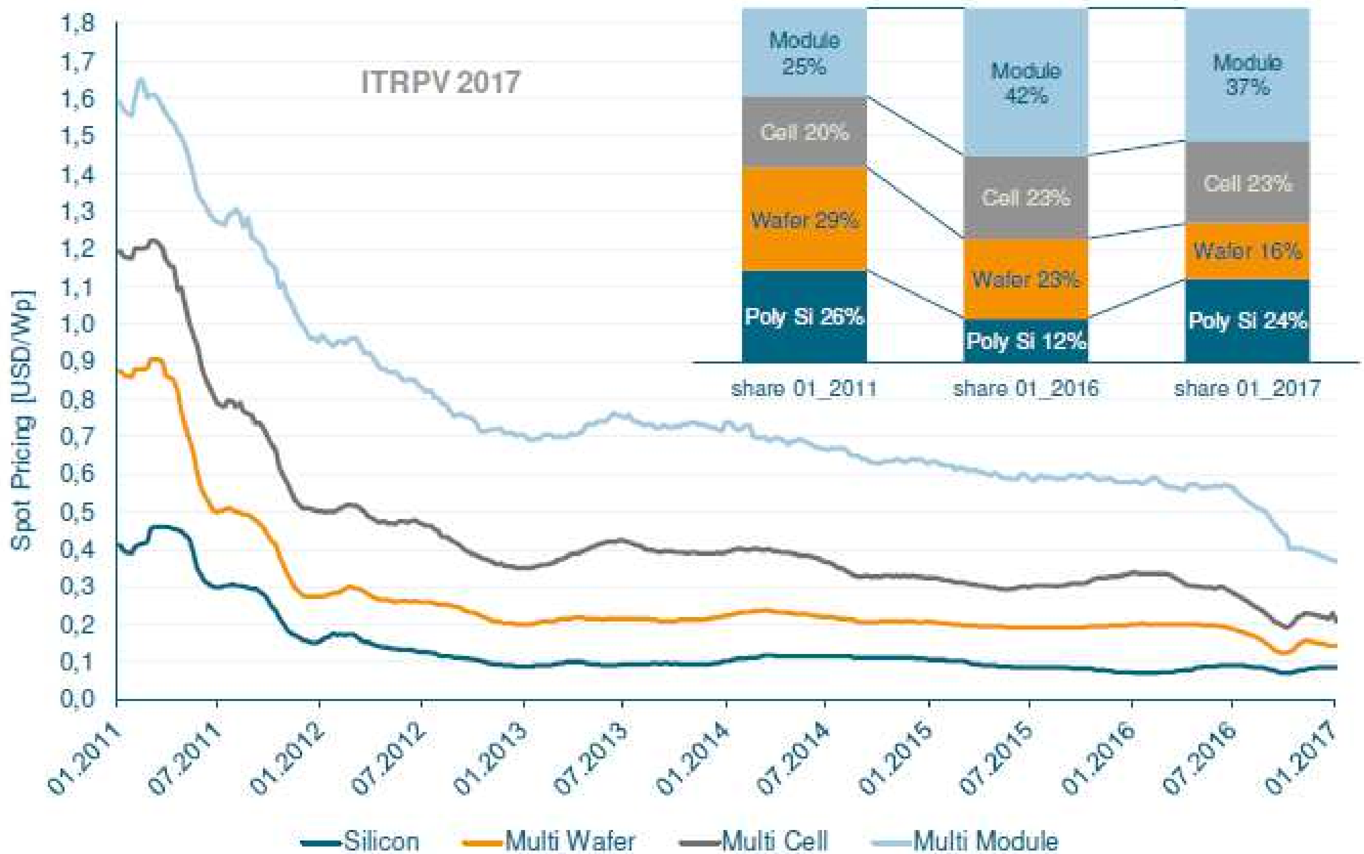
The value chain of crystalline silicon photovoltaics



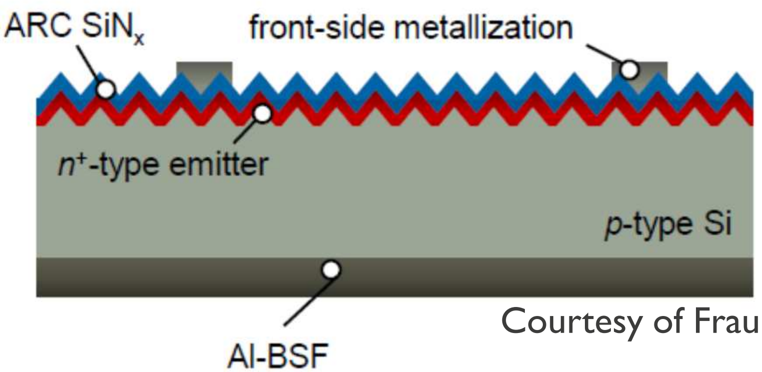
2 types of crystalline-silicon:
- Monocrystalline
- Polycrystalline

Courtesy of Al Hicks (NREL)

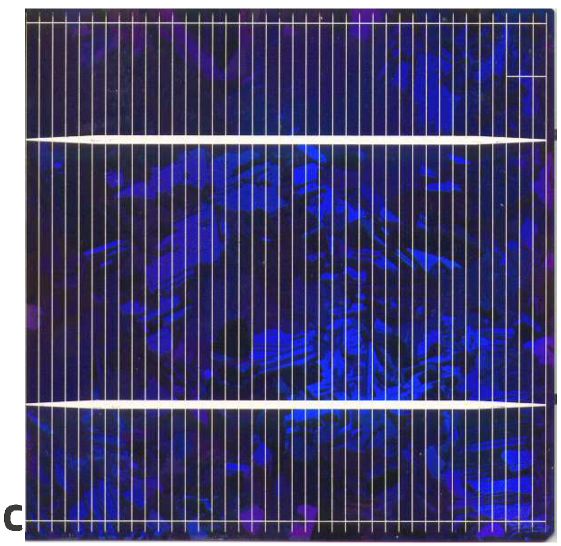
The cost structure of silicon modules



Most silicon solar cell production is based on the Al-BSF concept

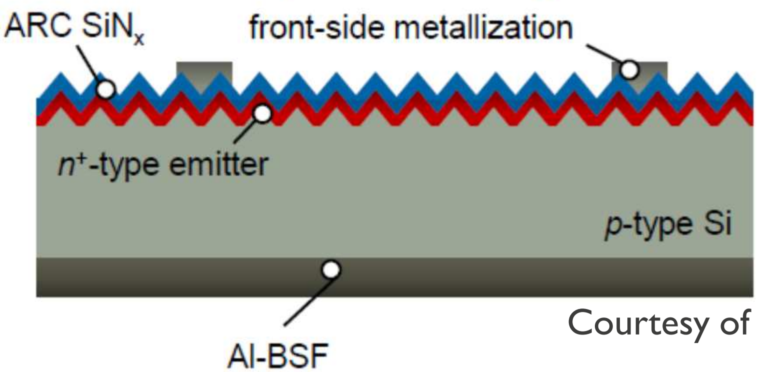


Courtesy of Fraunhofer ISE

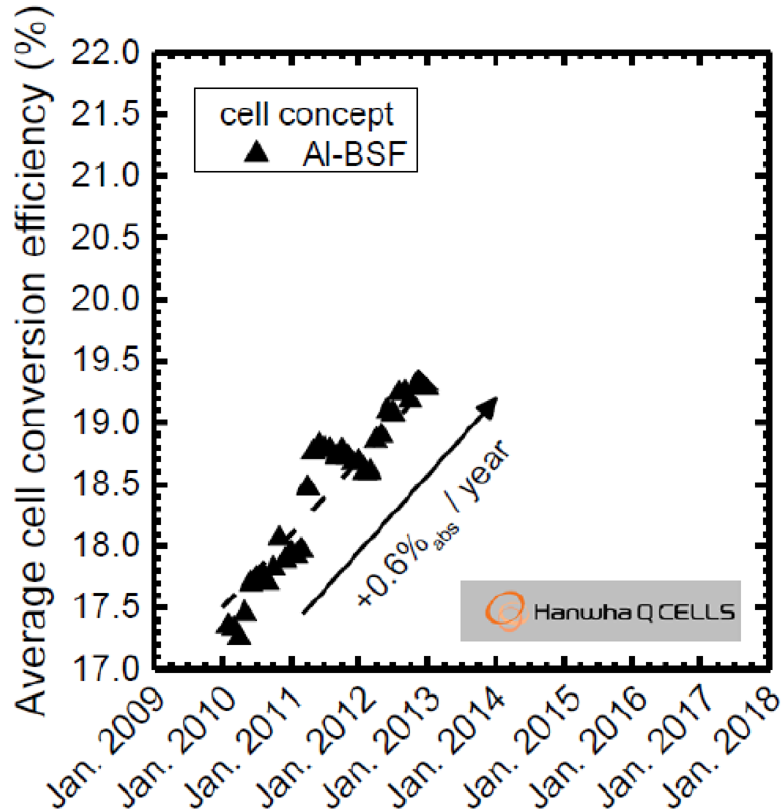


- Individual wafer (mono or multi)
- ↓ Saw damage removal + texturing
- ↓ $POCl_3$ Diffusion
- ↓ Parasitic Junction Removal
- ↓ PECVD SiNx:H ARC layer
- ↓ Screen Printed Metallisation
- ↓ Co-firing

The efficiency of industrial Al-BSF solar cells has been improved substantially over the years



Courtesy of ISE

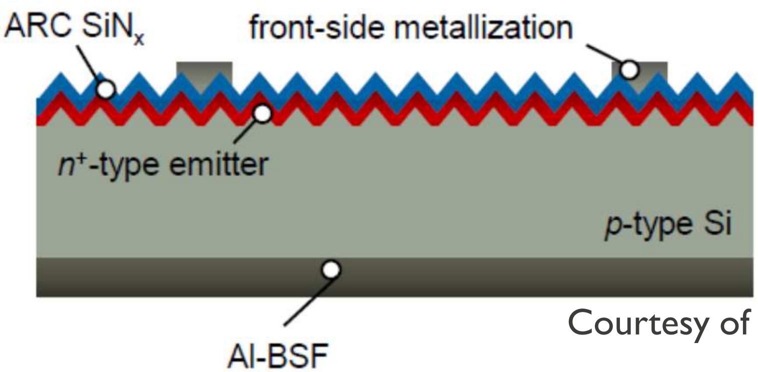


Average efficiency in production:

Multi ~ 16-18 %, Mono ~ 17-20 %

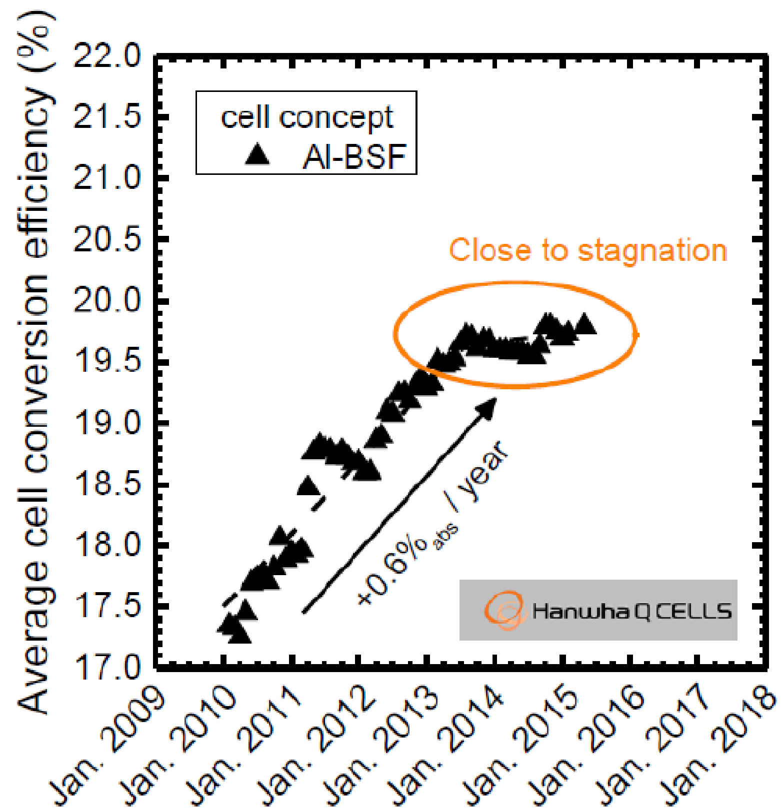
Fabian Fertig et al "***Mass Production of p-Type Cz Silicon Solar Cells …*** "
7th Silicon PV, Freiburg, Germany, April 3, 2017

The efficiency of industrial Al-BSF solar cells is limited due to the full-area metallized rear side



Courtesy of ISE

How can we further improve the industrial silicon solar cell efficiency and simultaneously reduce the cost?



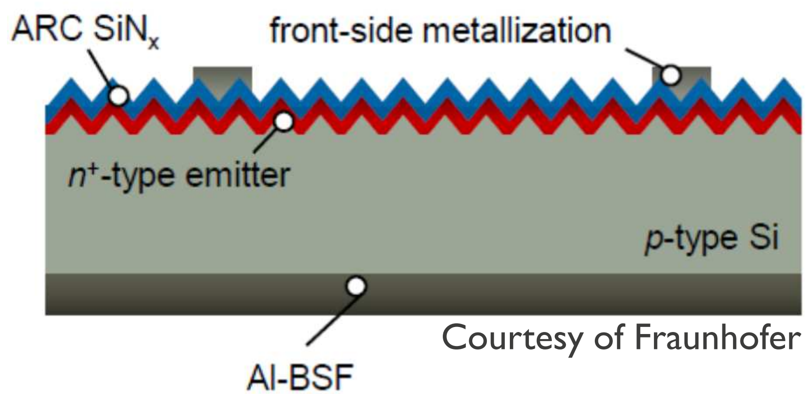
Fabian Fertig et al "*Mass Production of p-Type Cz Silicon Solar Cells …* "
7th Silicon PV, Freiburg, Germany, April 3, 2017

Main ways to further improve energy conversion efficiencies and reduce LCOE of crystalline-silicon modules

- Modifying the cell structure for higher cell efficiencies
  - PERC cells
  - Cells with passivated contacts
  - IBC cells
  - …
- Reducing material cost
  - Thinner wafers
  - Less use of Silver
  - Reduction of module material cost
  - …
- Increasing energy yield
  - Bifacial cells
  - …

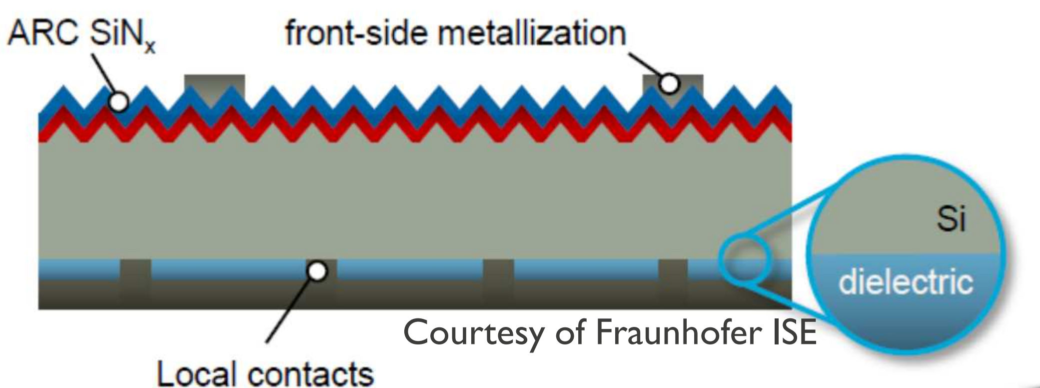
Novel cell structures for higher efficiencies

The PV industry is currently making the switch from Al-BSF to PERC-like solar cells



Courtesy of Fraunhofer ISE

“Standard cell”
Al-BSF



Courtesy of Fraunhofer ISE

“PERC cell”
Passivated rear contact

Two extra steps:

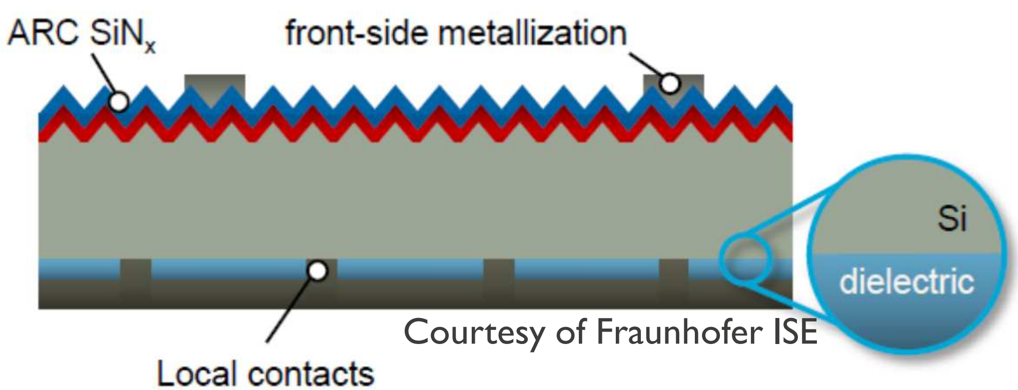
- Dielectric passivation on rear
- Local contact opening on rear

The switch to PERC cells allows the industry to continue to increase the cell efficiency year by year

Q.ANTUM = PERC cell of Hanwha Q Cells

Still 0.6 %abs /year increase

How far can we go like this?



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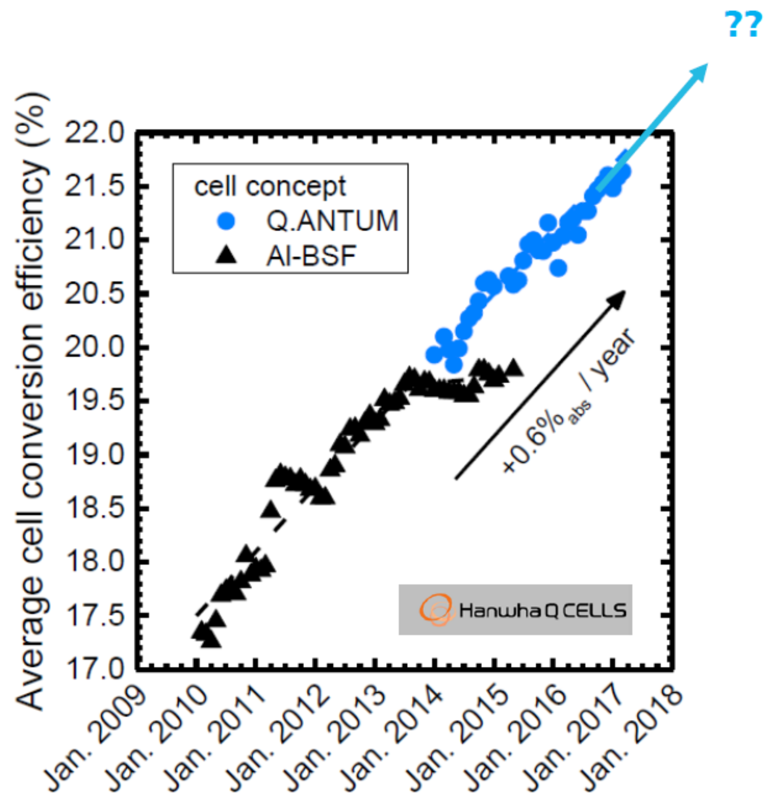

Fabian Fertig et al "*Mass Production of p-Type Cz Silicon Solar Cells …* "
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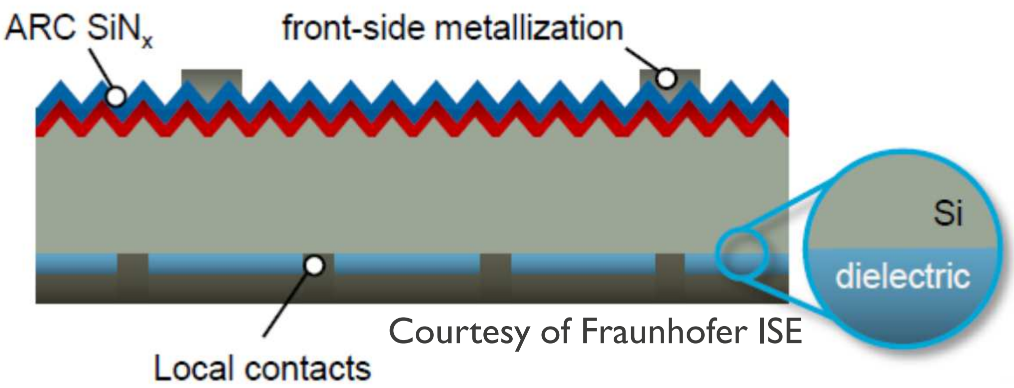
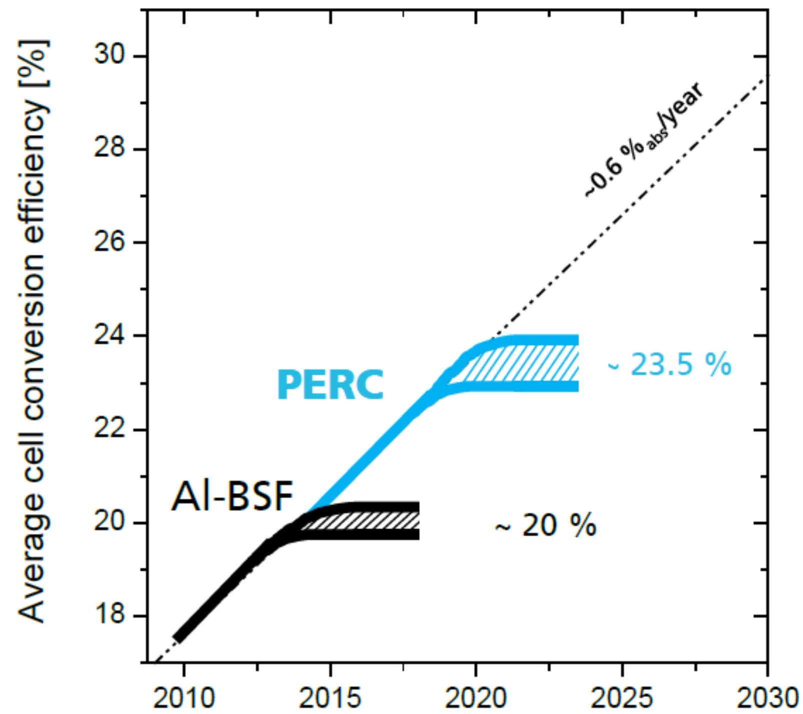
The efficiency of PERC cells is limited by contact recombination



Courtesy of Fraunhofer ISE

Further improvements possible by using passivating contacts and going to n-type silicon wafers.

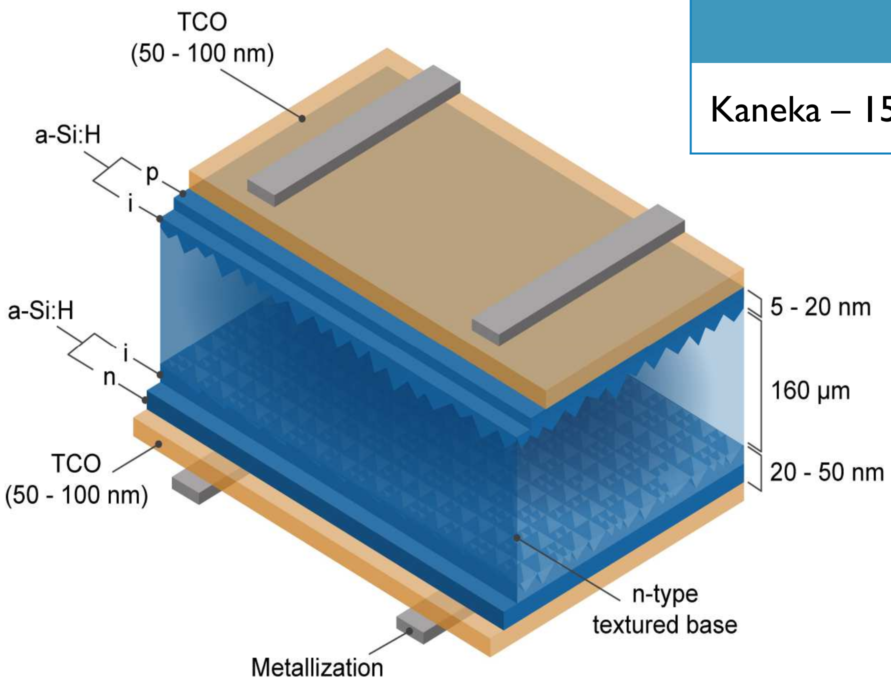


Courtesy of M. Hermle, Fraunhofer ISE

Two examples of cell designs with passivated contacts

1. Heterojunction cells

Best cell	J_{sc} [mA/cm²]	V_{oc} [mV]	FF [%]	Eta [%]
Kaneka – 152 cm²	40.8	738	83.5	25.1

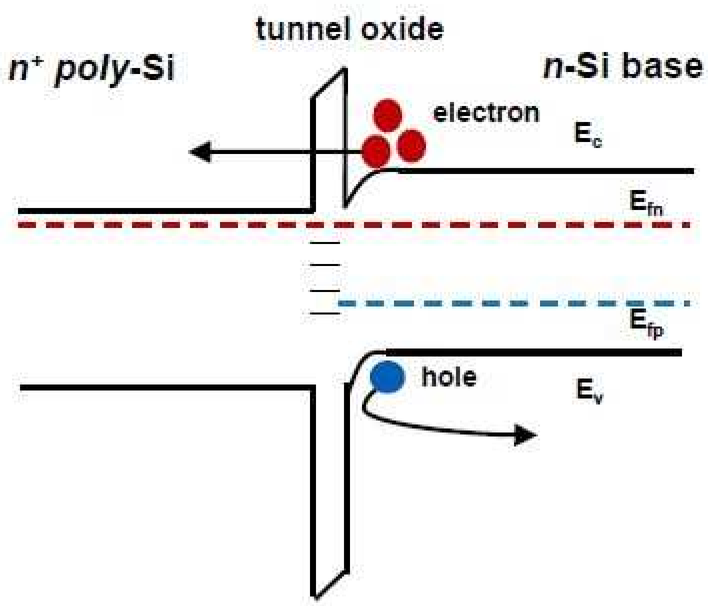


Courtesy of Al Hicks (NREL)

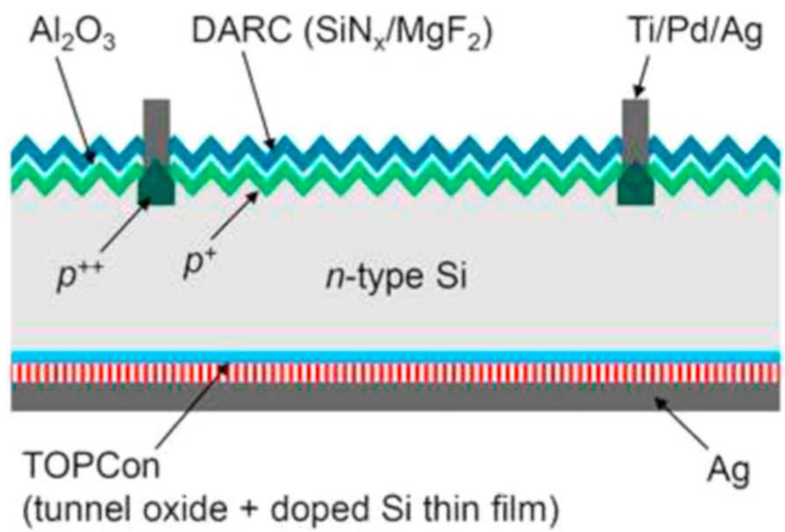
- n-type crystalline silicon absorber
- amorphous silicon doped layers for BSF and emitter
- Intrinsically highly efficient carrier selective contacts
- Originally developed by Panasonic (Sanyo)

Two examples of cell designs with passivated contacts

2. TOPCon cells



Courtesy of Fraunhofer ISE

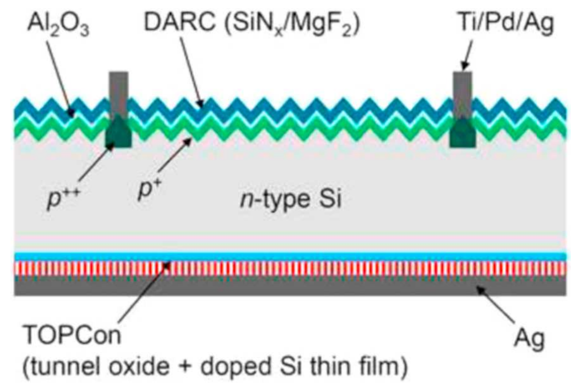


- n-type crystalline silicon absorber
- Tunnel oxide
- n-type doped polycrystalline silicon
- developed by Fraunhofer ISE

Two examples of cell designs with passivated contacts

2. TOPCon cells

Courtesy of Fraunhofer ISE



World record efficiencies obtained with this cell structure for:

- Multicrystalline silicon
- Monocrystalline silicon 2-side contacted cells

Best cells	J_{sc} [mA/cm²]	V_{oc} [mV]	FF [%]	Eta [%]
ISE – Mono 4 cm²	42.5	725	83.3	25.7[1]
ISE – Multi 4 cm²	41.1	674	80.5	22.3[2]

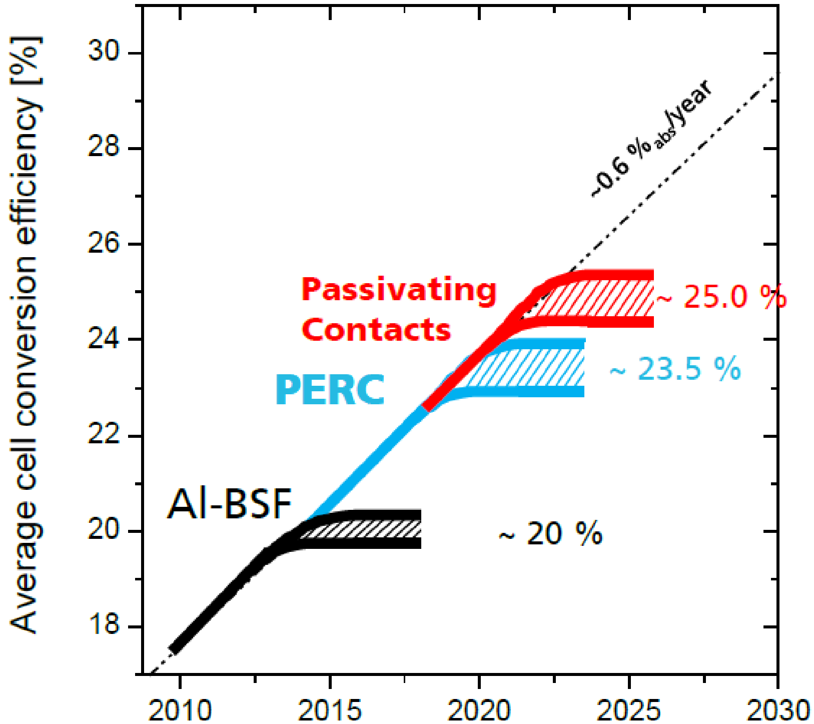
[1] Presented at SilcionPV conference 2017
[2] Presented at EU-PVSEC conference 2017

The efficiency of passivated contact solar cells is also limited

Physical limitations of passivated contact cells:

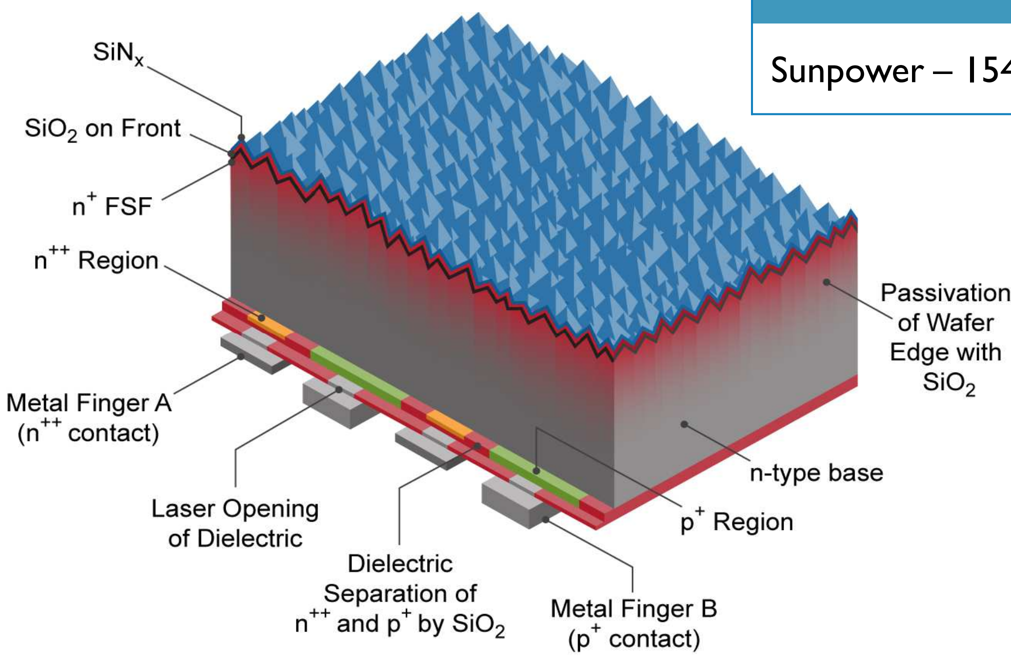
- Intrinsic Auger recombination
- Parasitic absorption
- Transport losses

Back Junction Back Contact solar cells!



Courtesy of M. Hermle, Fraunhofer ISE

Interdigitated back junction solar cells

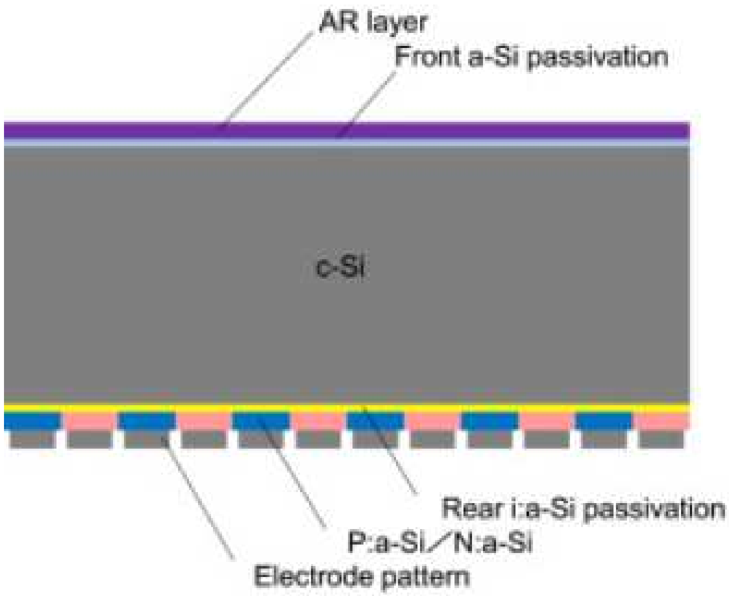


Best cell	J_{sc} [mA/cm²]	V_{oc} [mV]	FF [%]	Eta [%]
Sunpower – 154 cm²	41.3	737	82.7	25.2

- n-type crystalline silicon absorber
- emitter and BSF regions at rear
- all contacts at rear side
- less shadowing losses on front
- more complicated processing required

Courtesy of Al Hicks (NREL)

Combining the best of both worlds: heterojunction IBC devices



Courtesy of Kaneka

- n-type crystalline silicon absorber
- emitter and BSF regions at rear made by a-Si:H
- all contacts at rear side
- less shadowing losses on front
- more complicated processing required

World record efficiency obtained with this cell structure for crystalline silicon:

Best cell	J_{sc} [mA/cm²]	V_{oc} [mV]	FF [%]	Eta [%]
Kaneka – 180 cm²	42.5	740	84.7	26.6

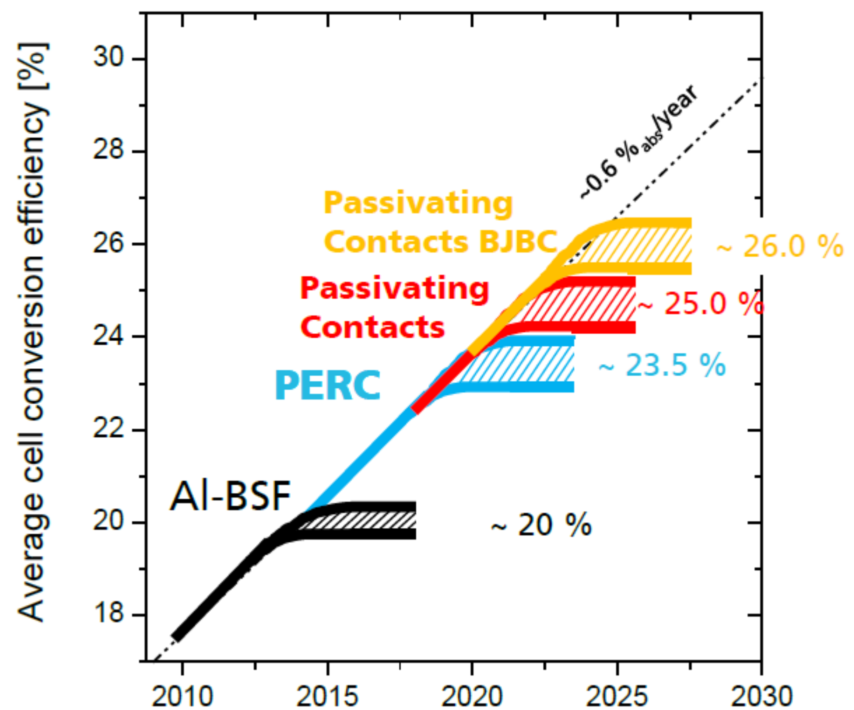
Presented at SilcionPV conference 2017

A crystalline silicon solar cell structure roadmap

Physical limitations still remaining:

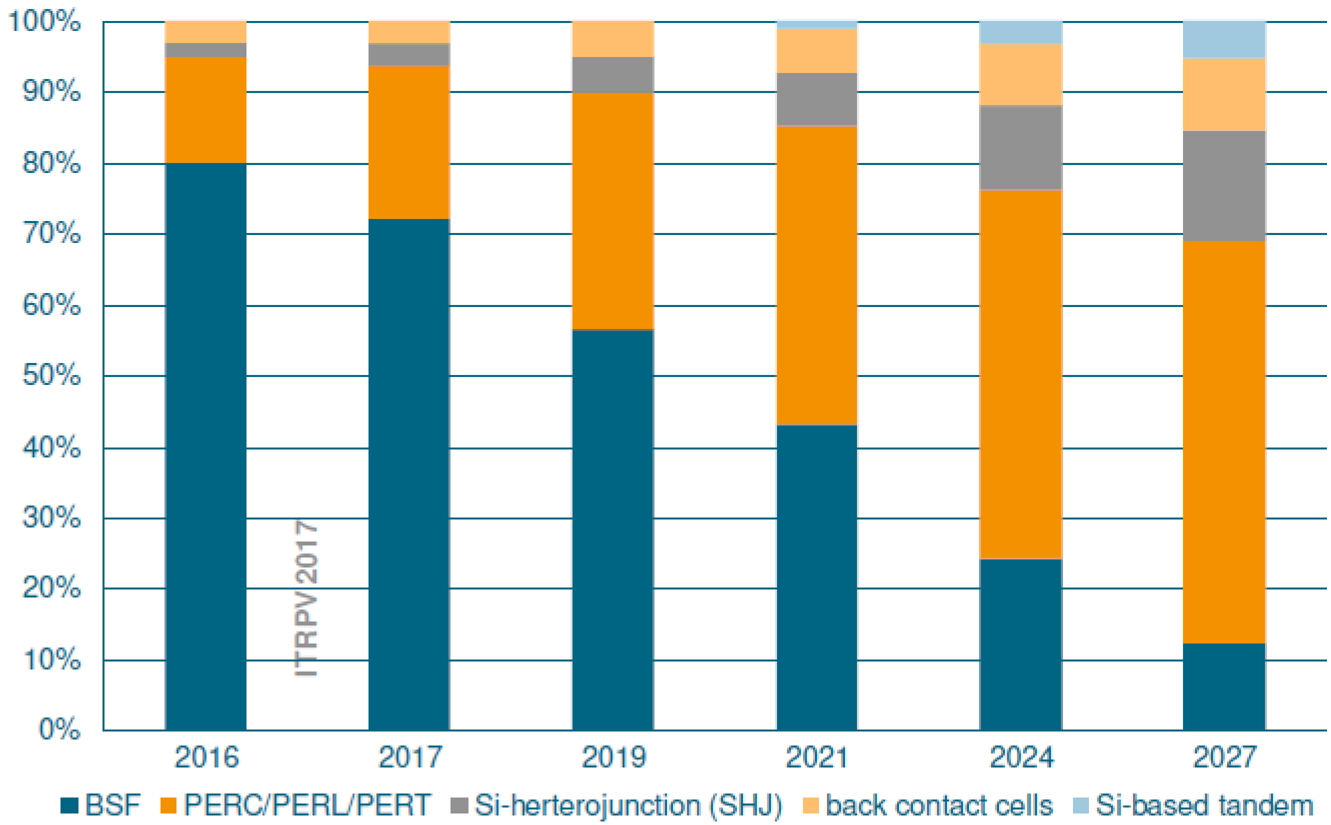
- Intrinsic Auger recombination
- Imperfect light trapping
- Transport losses

Further efficiency improvements will require tandem devices



Courtesy of M. Hermle, Fraunhofer ISE

The market share of these novel cell designs is expected to increase substantially in the coming years



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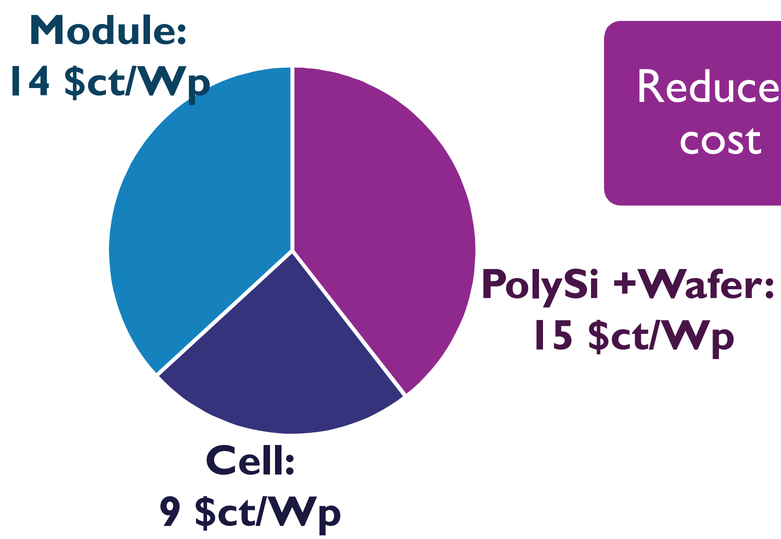
Reducing material costs

Decreasing the wafer thickness can lower the cost of Silicon modules

Cost Si wafer is > 35% of total module cost

(current common thickness 180 um)



ITRPV, March 2017

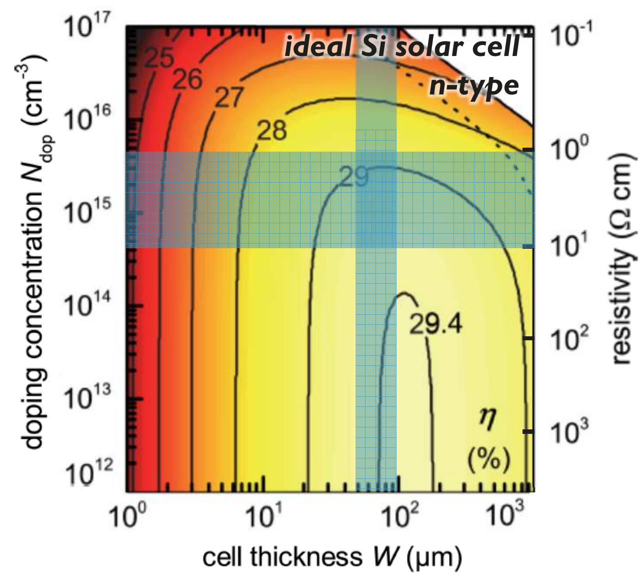
Solar cells on thin c-Si wafers

Reduced cost

Increased efficiency

Theoretical max eta for 50-100 um

(for common base doping of 1-10 Ohm.cm)



Richter et al., IEEE Journal of PV (2013)

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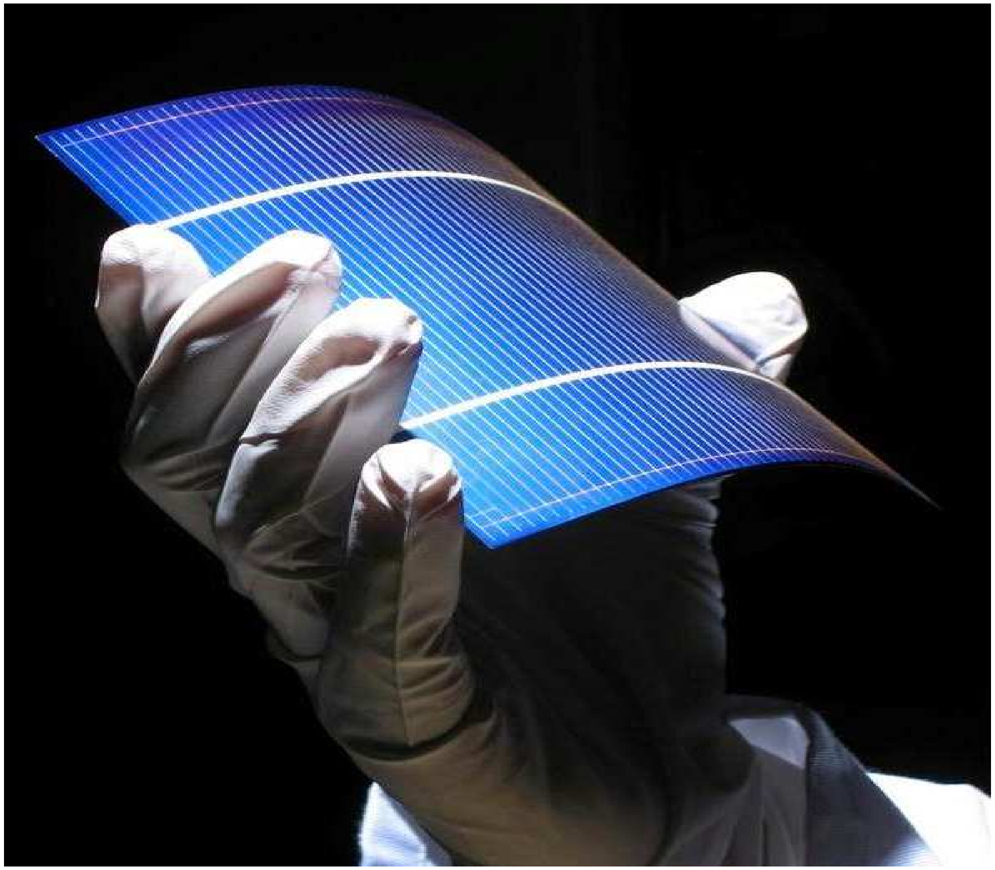
Decreasing the wafer thickness can open up the way for novel applications



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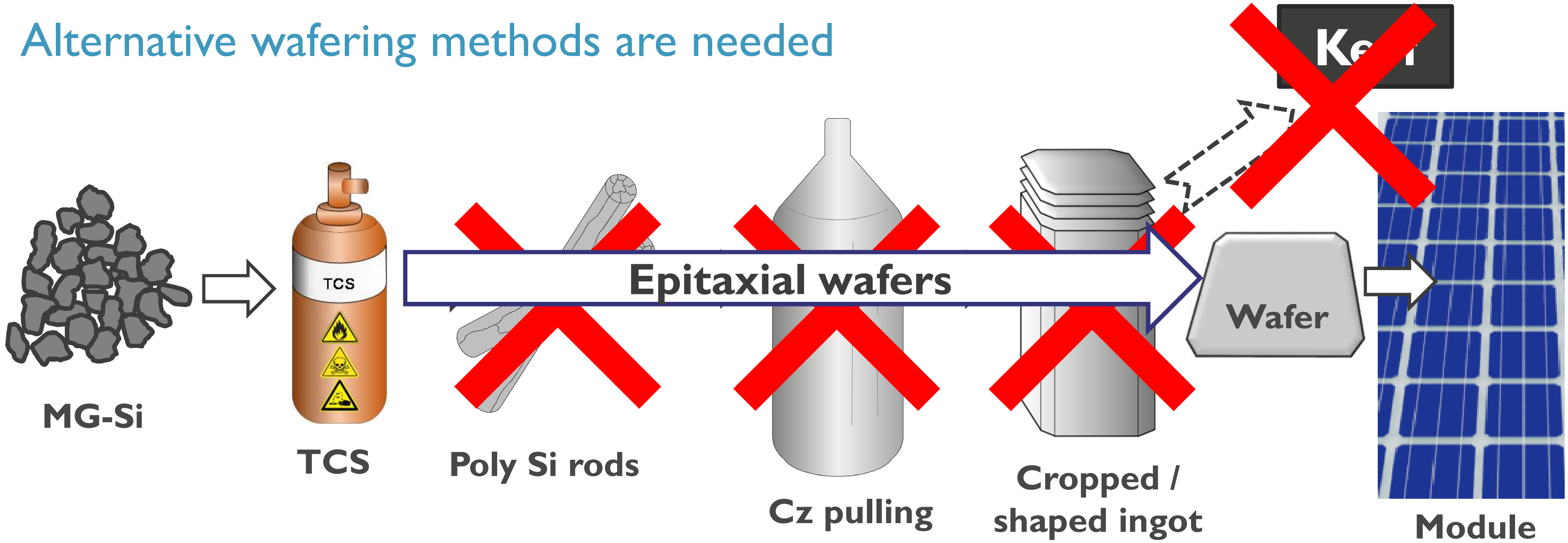
Alternative wafering methods are needed



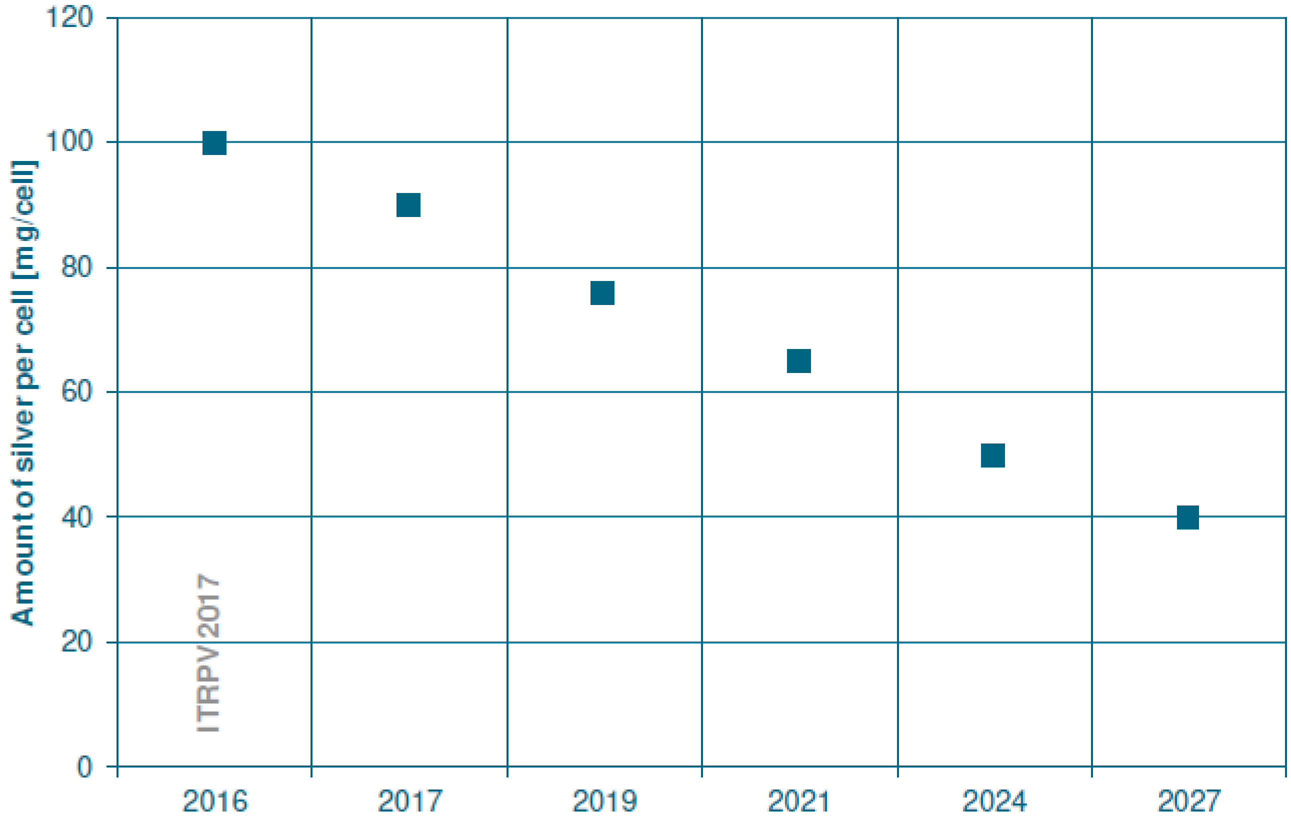
③ **Direct growth of wafers from gas-phase:**
Epitaxial lift-off

② **Direct crystallization of wafers from melt:**
Ribbon growth
1366 Direct Wafer™

① **Kerf-free wafering of Si ingots:**
Stress-induced lift-off
Implantation-based lift-off

imec EnergyVille

The industry foresees also a further continuous reduction of the amount of Silver used per cell

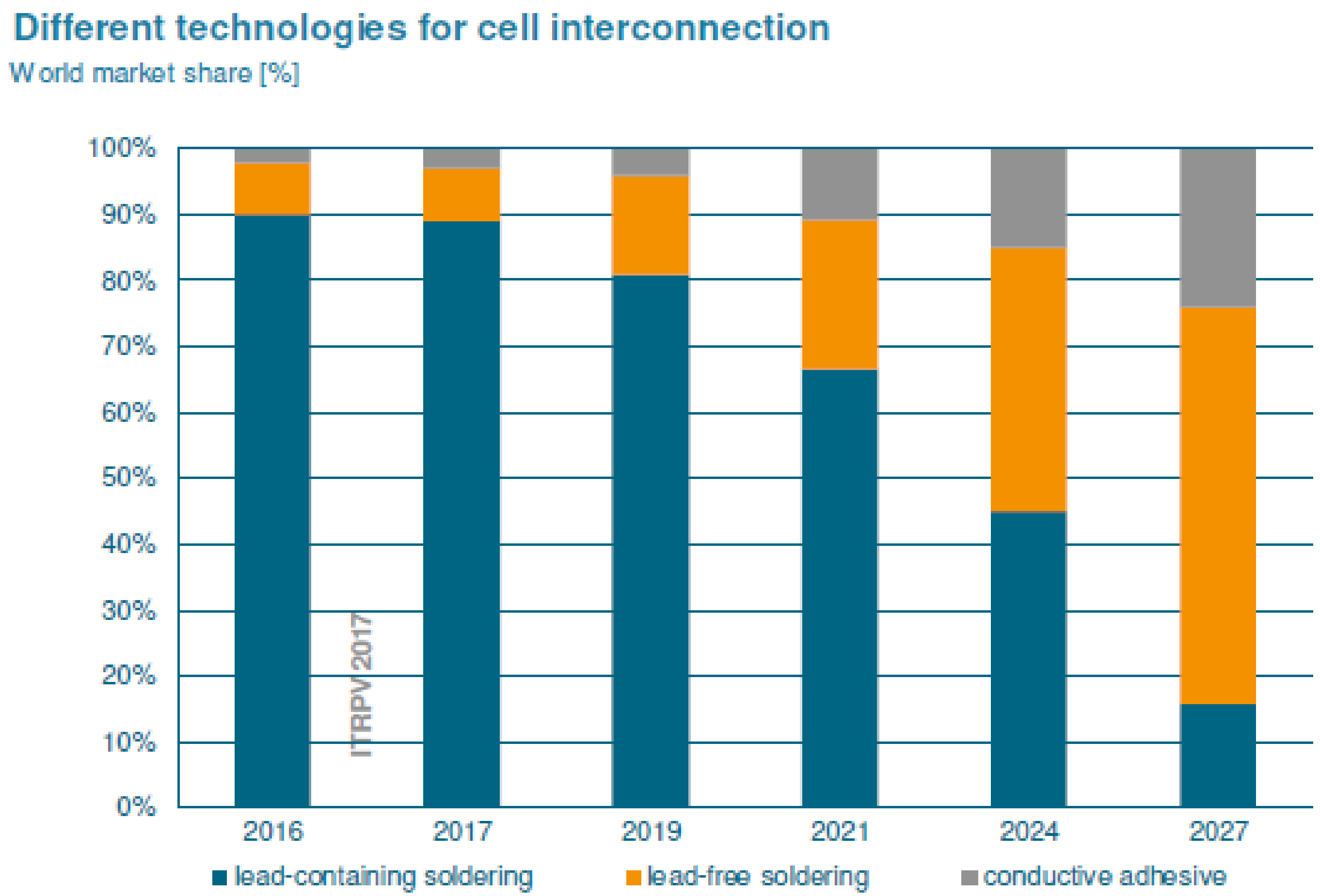


Ag cost amounts to ~ 8% of cell cost

Requires new developments in pastes and screens

Cu plating is also being looked at as alternative

Adapting and reducing the cost of module materials is also very important



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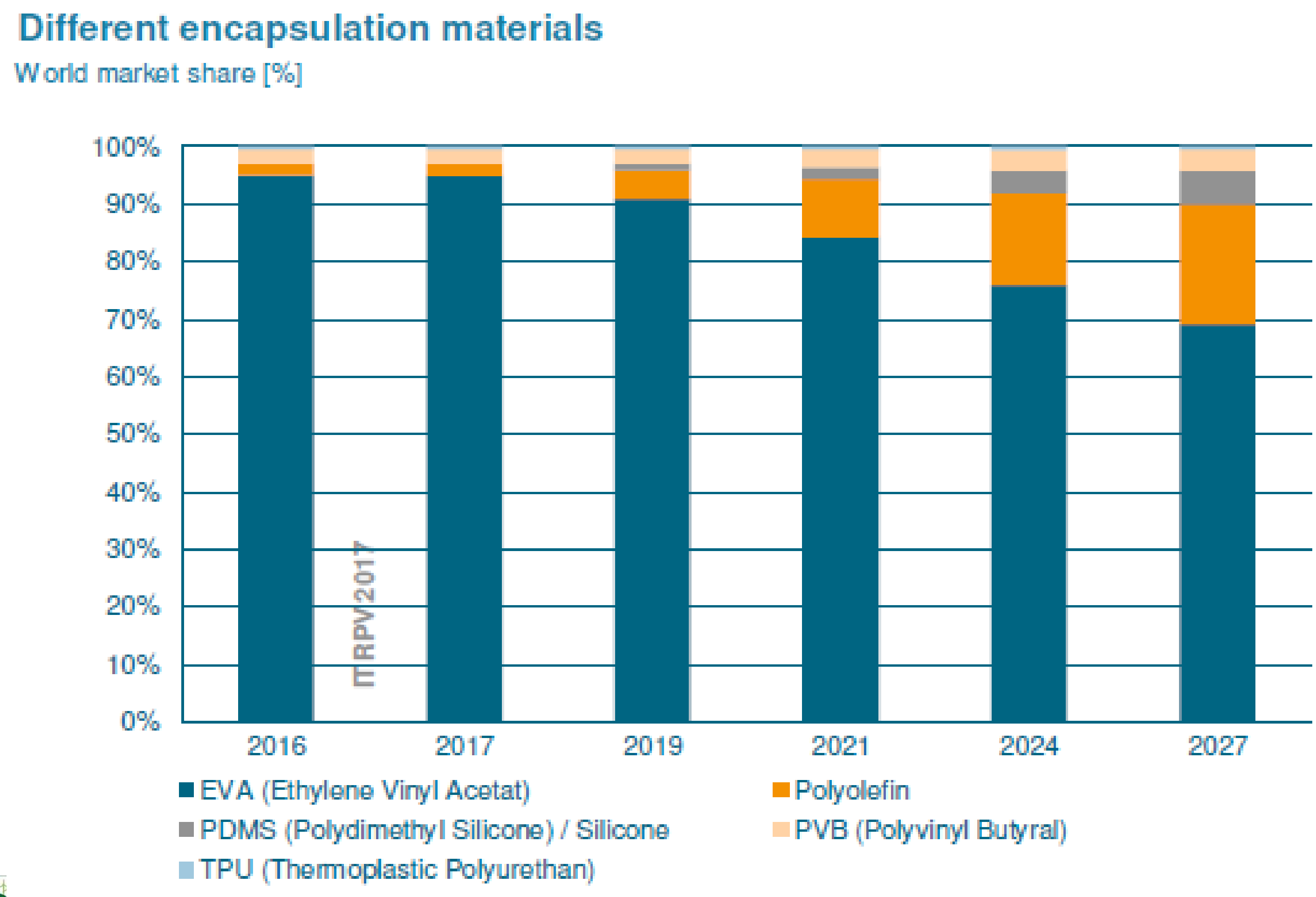

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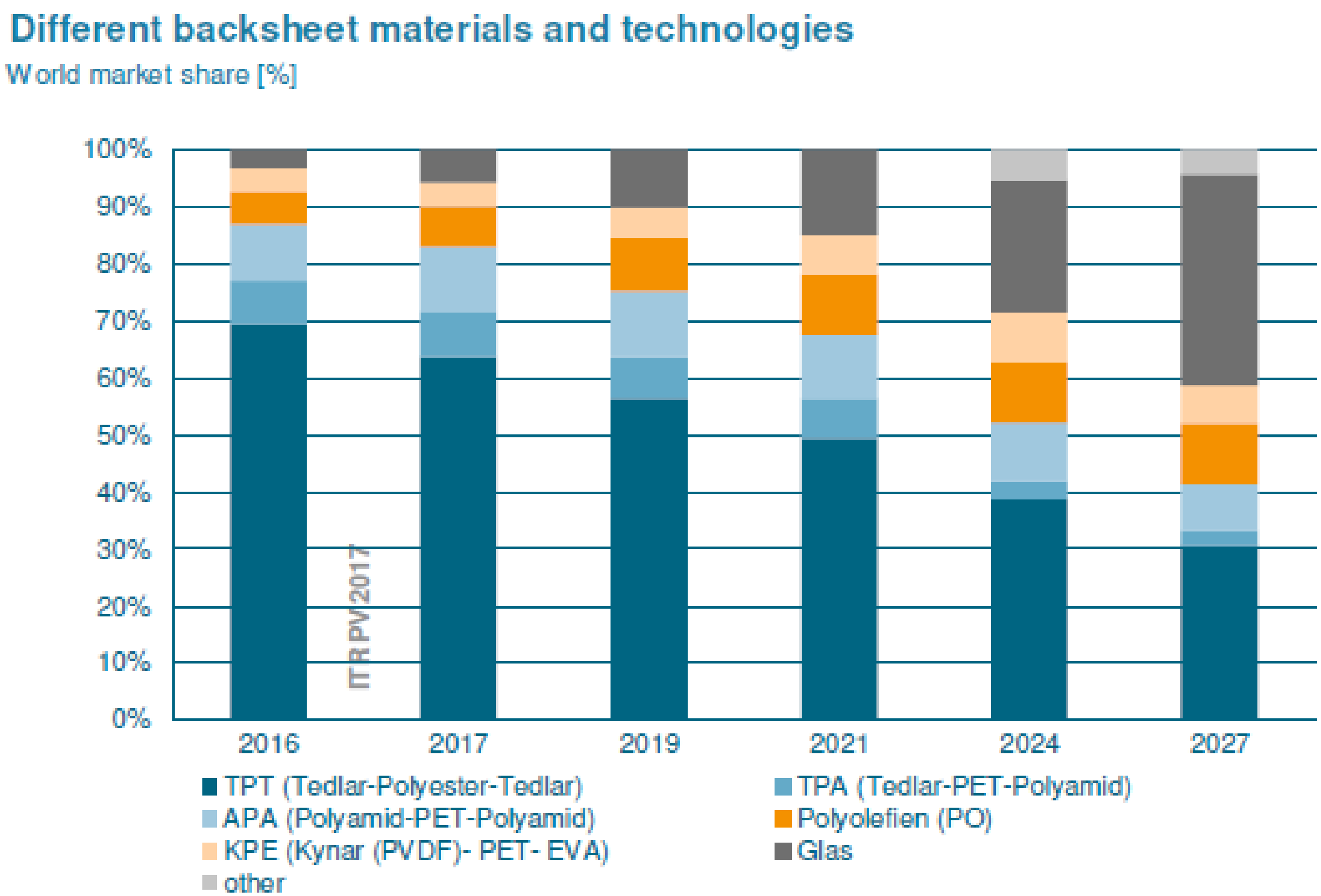

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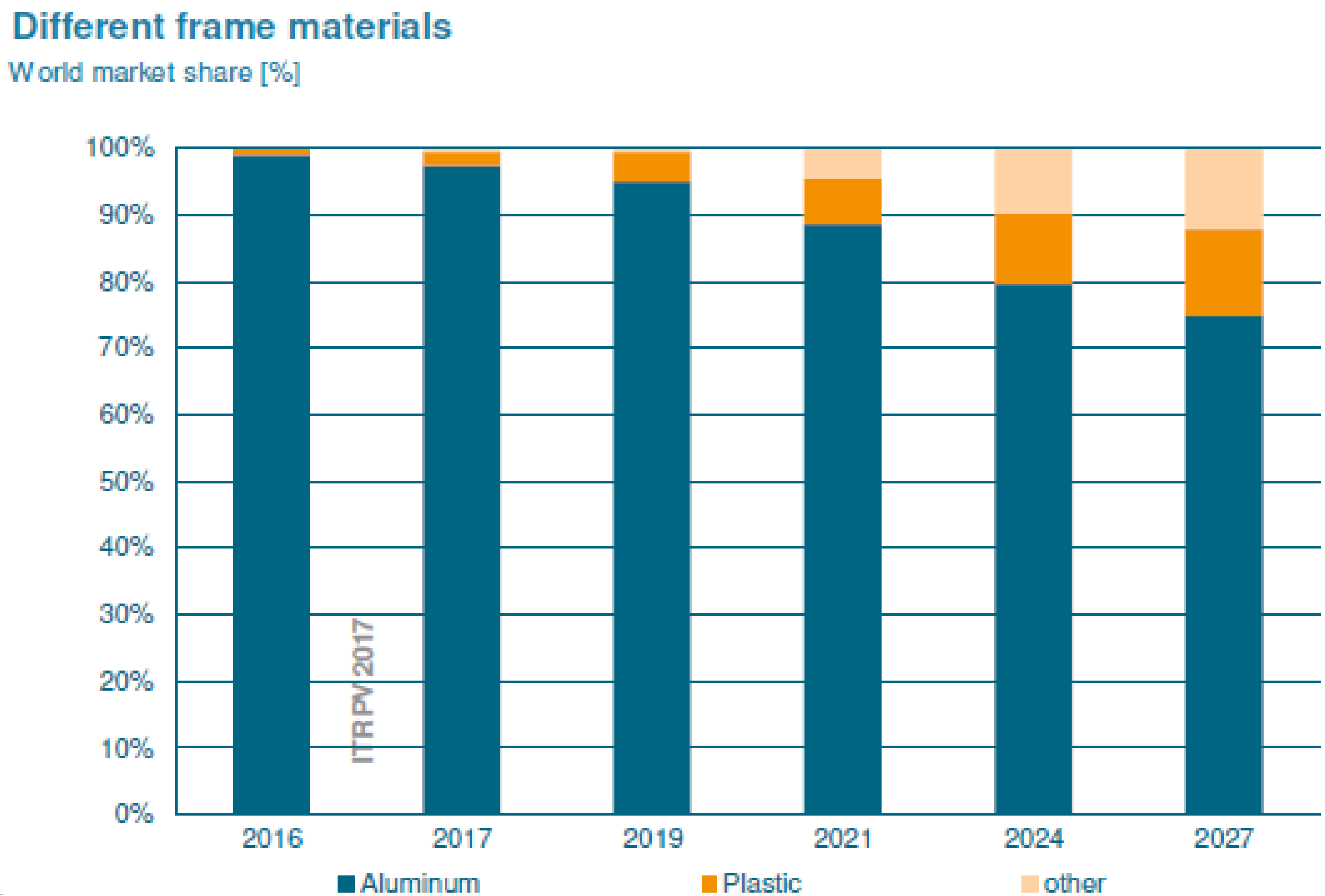

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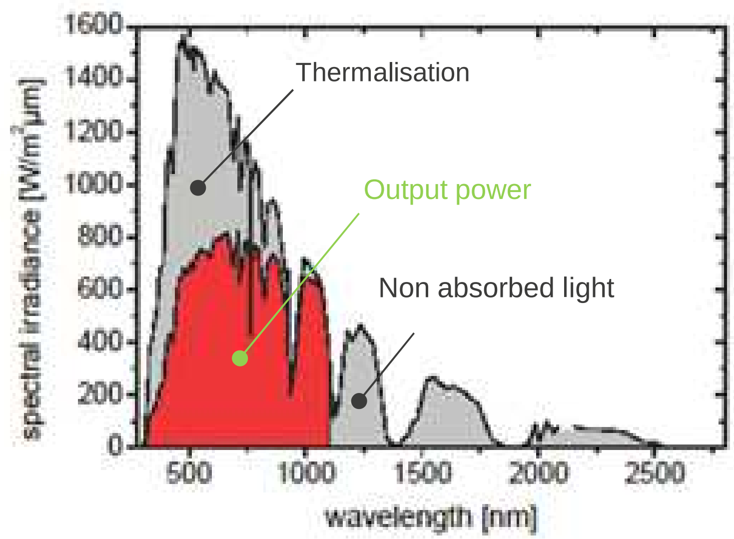
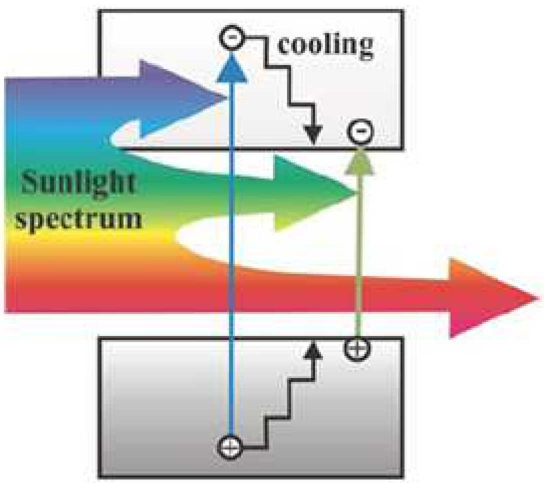
Tandem devices with silicon bottom cells

The theoretical efficiency limit of a single junction silicon solar cell is 29.4%

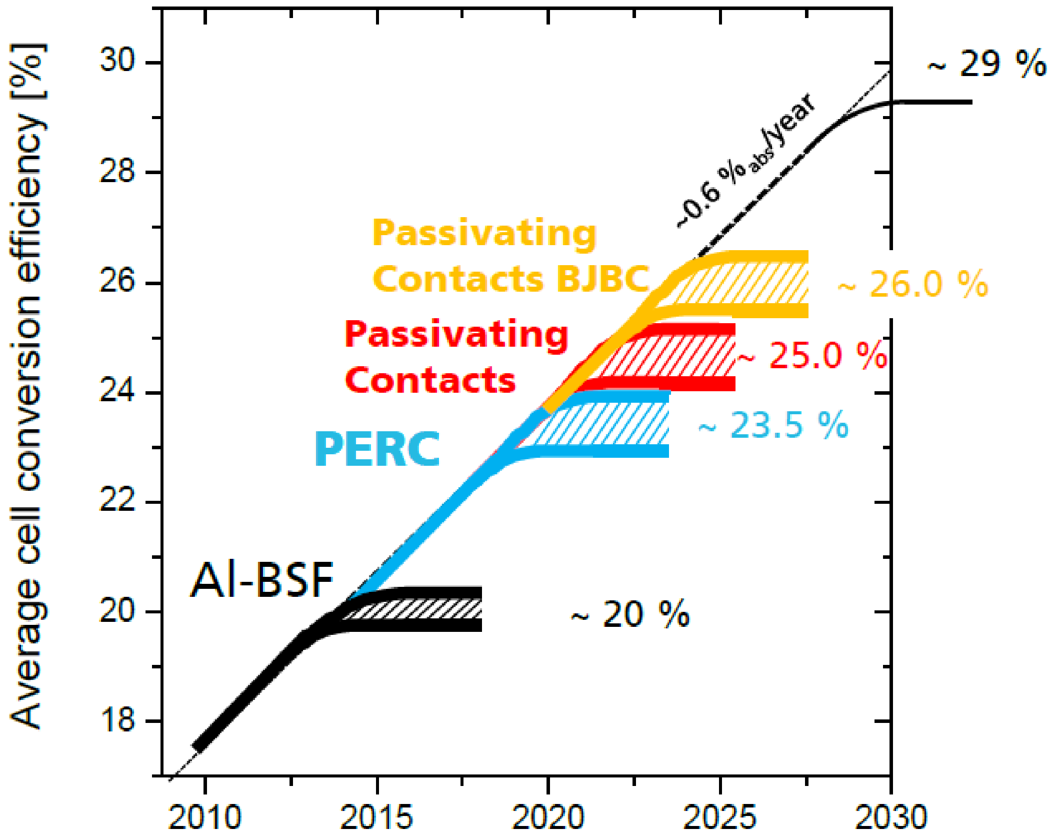
Auger limit of single-junction silicon solar cell is 29.4%

Limitations by thermalization and transmission





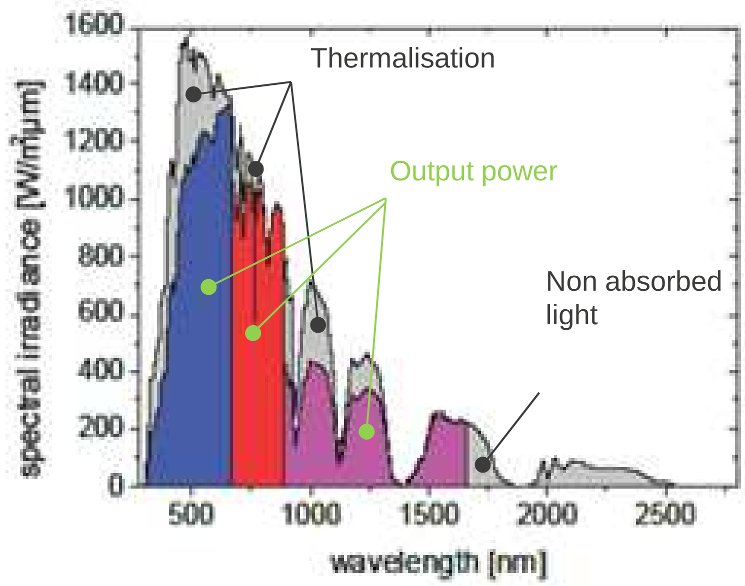
Will this limit mean the end of silicon solar cell technology?

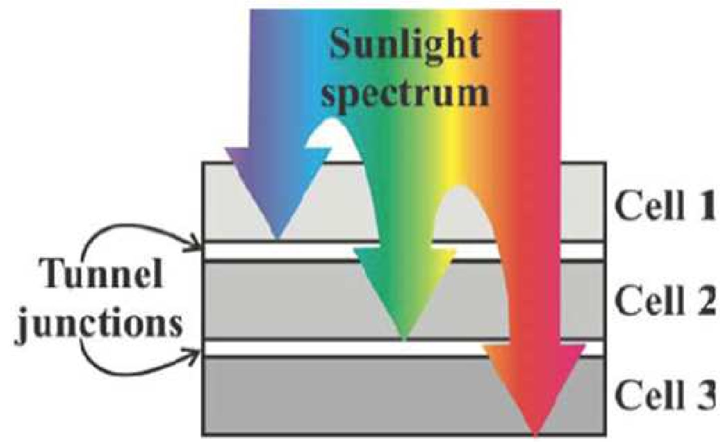


Courtesy of M. Hermle, Fraunhofer ISE

Crystalline-silicon based multi-junctions will allow to push efficiencies above 30%

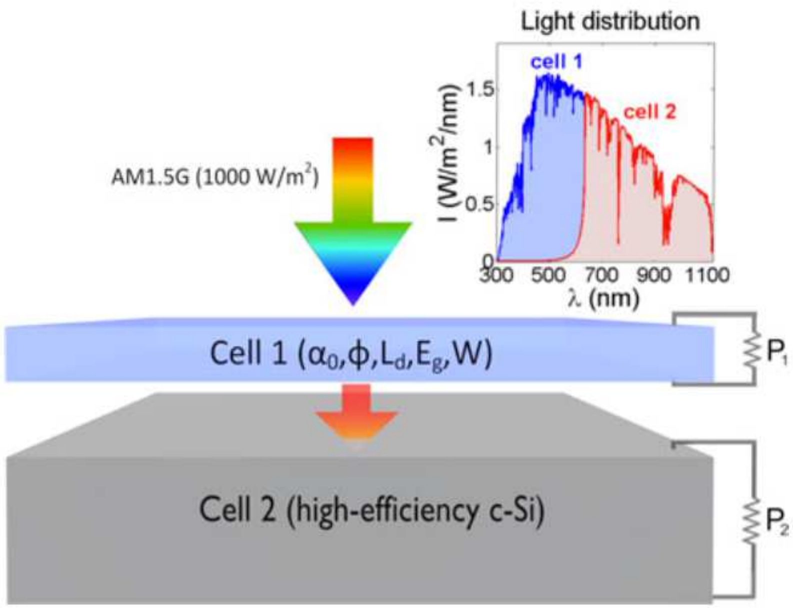
Multi-junction cell concept:

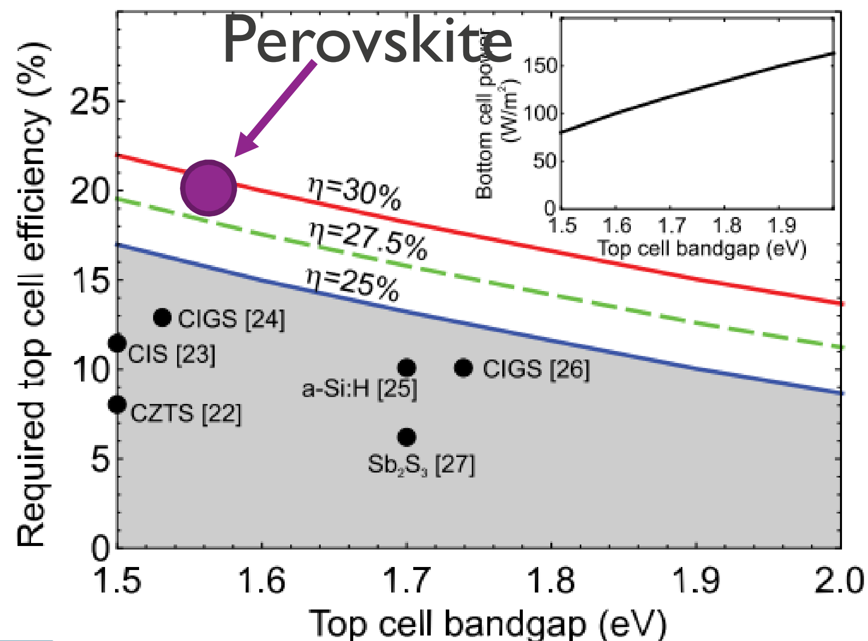




Note: multi-junction with two cells is called tandem

Crystalline-silicon based tandem devices

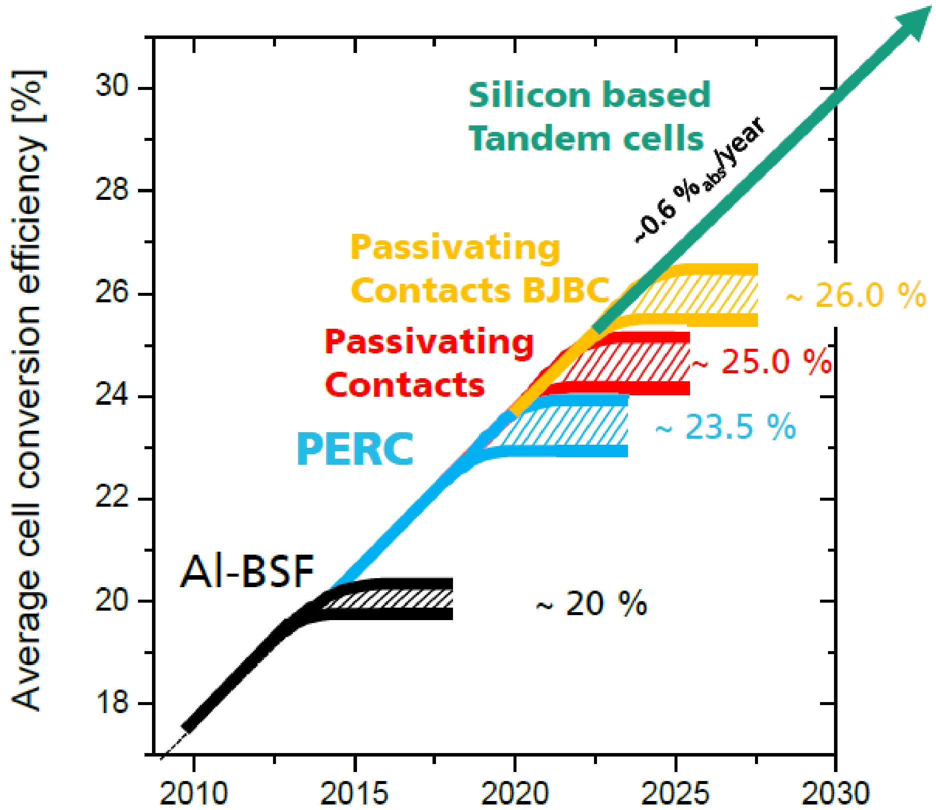




Needed: thin-film top cell with high bandgap, high efficiency, and minimal sub-bandgap absorption

T. P. White, IEEE J. PV, Jan. 2014

Silicon-based tandem devices will ensure that silicon solar cell technology still has a long and bright future



Courtesy of M. Hermle, Fraunhofer ISE

Conclusions

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- Silicon wafer-based modules dominate the PV market and will continue to do so
- New cell structures with high industry potential are being developed to increase efficiency and reduce the levelized cost of electricity
- The cost can be further reduced by dedicated material research leading to reduced material usage or novel low-cost materials
- Tandem devices will be the way towards silicon-based module efficiencies above 30% but substantial material research will be needed for the top cell

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